Diyala Journal of Engineering Sciences

Journal homepage: https://djes.info/index.php/djes

ISSN: 1999-8716 (Print); 2616-6909 (Online)

High Performance IIR Filter Design Based on Fast Multiplier

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ARTICLE INFO

Article history:
Received September 7, 2024
Revised December 18, 2024
Accepted December 23, 2024
Available online Maech 18, 2024

Keywords:

IIR filter
FPGA
HDL
BCD multiplier
Mux-Multiplier

ABSTRACT

This paper presents an optimal new method to design infinite impulse response (IIR) digital filters through implementing and comparing various multiplier architectures in order to opt the best approach among them. The reason behind focussing on the multiplier unit belongs to its essential role in the performance of the IIR filters. Direct form II is the realization form opted to characterize the suggested IIR filter which is coded, using Quartus II software and subdued to gate level simulation on field programmable gate array (FPGA) kit board. The proposed IIR filter, whose architecture includes the binary coded decimal (BCD) involved in it, has gained the best outcomes. The BCD multiplier is compared to other multipliers such as: array multiplier, parallel multiplier with two-splitting of Booth and parallel circuits, Vedic multiplier and Mux-Multiplier which are implemented with the Cyclone IV GX FPGA kit platform. It was observed that BCD-multiplier has recorded the smallest logic elements (188) along with the fastest operation speed (282.8 MHz) and the lowest delay time (7.89 ŋSec) compared to other approaches. The IIR filter circuit designed with the BCD multiplier is programmed and implemented on the Cyclone IV GX FPGA kit platform. Depending on the obtained results, the IIR filter based BCD-multiplier has promising features that make it more attractive than IIR systems based on other multipliers. Moreover, these features make the IIR filter widely exploited in diverse electronic systems and devices such as: images and biomedical signal processing applications, communications and radar systems.

1. Introduction

Recently, digital signal has no doubt to prove its significance in human beings since it has been involved in providing more comforts in their daily life [1]. Basically, a filter system is of the main systems being exploited which is defined as a device that suppresses unnecessary electrical signals in order to ensure passing the wanted portion of the filtered signals [2, 3]. Digital filter has been regarded as an important unit due to its crucial role in every signal processing system. Generally, there are two types of digital filters known as the finite impulse response (FIR) and the infinite impulse response (IIR) filters. Within digital filters many performance specifications, that would be regarded too difficult with analogue filters, are significantly avoided in digital filters [4]. IIR filter is one of the well-known filter types that has an infinite number of nonzero terms and response impulse of infinite duration [5]. Due to the small sizing and few coefficients requiring in IIR filters, they are widely involved in fast systems with many applications of various majors such as in communications, control and electronics [6]. For instance, in biomedical signal processing, digital filters have an essential role in reducing the noise artefacts which might come with bio-signals such as the case of myoelectric signals [6].

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DOI: 10.24237/djes.2025.18111

The field programmable gate array (FPGA) technology has been presented in various aspects of industrial areas. The fast response of FPGA-based designed systems offers an effective reason to apply it in digital real-time applications [7]. The wide capacity of FPGA parallel processing along with its wide data width flexibility enrich the systems with strong and robust property [8]. Having been utilized extensively, digital filters designed in FPGA can be found in many areas such as in image processing and biomedical signal processing and else [9].

A series of recent studies has indicated the design and implementation of digital IIR filter using different techniques. Booth multiplier is used in [10] to design and implement IIR in FPGA environment. Another technique presented in [11] suggested the design of a real-time temporal IIR digital filter for stimulus artefact rejection (SAR). Also, XILINX FPGA board was used to propose the digital IIR filter architecture discussed in [12] where the gate level design was chosen to implement the filter through analysing its impulse response. Moreover, the study of [13] has discussed the method of state-space representation using MATLAB to implement a 4th order low-pass Butterworth digital IIR filters. In [5], designing of direct form and transposed of direct form FIR and IIR filters is done in FPGA. The design aims to analyse the filter performance with respect to amount of both the time delay and execution period as well as providing low area size and low power with a high-speed implementation in return. In order to attenuate the accompanied noise artefacts of myoelectric signal network, there was a method in [14] by which IIR filter is implemented through utilizing the Xilinx IP Core for multiplication (Multiplier-Adder).

Implementation of fast IIR filter on FPGA through the concept of look-ahead arithmetic was discussed in [15]. After preparing filter coefficients using MATLAB, Xilinx system generator was used to implement the digital filter [16]. In [17], a notch / anti notch IIR filter of order 2 is discussed by applying floating point arithmetic architecture which was implemented on FPGA platform. The author presented a mixed technique to minimize the design complexity along with obtaining an ability to control filter parameters for better performance in terms of delay and frequency of tuning. In [18], using VHDL language was taken as a way to design and implement digital IIR filter regardless to the editor and simulator. Instead of multipliers, the author used a group of digital adders to simplify the multiplication processes in order to boost the IIR filter speed. Differently, MATLAB based FPGA implementation of 4th order IIR low pass filter is proposed in [19] to obtain fast speed of FPGA performance. Gravitational Search Algorithm Biogeography Based Optimization (GSA- BBO) was used to design an 8th order IIR band stop filter (BSF) and band pass filter (BPF) as in [20]. In [21], IIR filter design was enhanced by avoiding the use of hardware multipliers and using series of adders in order to decrease number of filter coefficients in the system transfer function. Also, the study of [22] have discussed the design of digital IIR filter where an FIR based IIR filter implementation is performed on FPGA platform in order to obtain reduction of computing time and power and improvement of operating speed. In [23], a hybrid approach is illustrated for the aim of implementing a various orders FIR and IIR LPF filter through coupling between MATLAB and FPGA. Also, an ECG signal de-noising IIR and FIR digital filter with optimal order was presented in [24] by transforming IIR digital filters prepared in MATLAB into a Verilog code through HDL programming commands which led to a better performance than MATLAB in terms of power consumption and chip size-area. Enhancing the performance of MOSFET transistors, as discussed in references [24, 26], and [27], can effectively improve the IIR filter circuits.

Hence, improving the efficiency of the IIR filter can be achieved by developing the performance of the multiplier circuit which is particularly beneficial in multiple scenarios such as basic digital signal processing, small-scale arithmetic operations, filters and signal analyzers in real-time systems and medical imaging devices (Magnetic Resonance Imaging (MRI) or ultrasound).

In this paper, multiple architectures have been utilized to implement the multiplier circuit

which is an essential part in digital IIR filter systems. The proposed design aims to opt and candidate the optimal multiplier architecture among group of multipliers. All compared IIR based multiplier circuits were implemented using FPGA environment.

The aim of the research is to design and HDL programming various multiplier architects so as to identify their advantages through establishing a comparison in operating speed, delay time and the required logic elements. Depending on the obtained results, the most optimal multiplier architect can be specified to be applied in the destinated IIR filter system.

The outline of the paper is organized as follows: section 1 provides the introduction and the previous work survey. Section 2 describes the theory of IIR filter. Section 3 contains design of the proposed IIR filter circuit. Section 4 presents the multiplier circuit design techniques. Section 5 demonstrates results and discussion. Finally, the conclusion and future work is presented in the section 6.

2. Infinite Impulse Response (IIR) filter

The IIR filter is also known as the recursive filter due to the existence of feedback in its transfer function which in return has both of zeros and poles in its mathematical expression. On the other hand, digital FIR filters have only zeros in their transfer function. Mathematically, the transfer function of IIR filter consists of numerator and denominator from which zeros and poles are derived respectively [23]. The difference equation of digital IIR filter is given in Equation (1). It is clearly shown that the transfer function of the IIR filter has a feedback path because of the shifted samples of output signal. Hence, the output y[n] depends on samples from its previous status as well as the present states of the input [5].

$$y[n] = \sum_{k=1}^{M} A_k x(n-k) - \sum_{k=0}^{N-1} B_k y(n-k) \quad (1)$$

Where, B_k refers to zeros' coefficients and A_k refers to poles' coefficients. The filter order is denoted by upper limits indexes denoted as M and N in the summation.

In Z-domain, the linear time-invariant causal digital IIR filter transfer function can be expressed in the following form shown in Equation (2).

$$H(z) = \frac{B_0 + B_1 Z^{-1} + B_2 Z^{-2} + \ldots\ldots B_M Z^{-N}}{1 + A_0 + A_1 Z^{-1} + A_2 Z^{-2} + \ldots\ldots A_N Z^{-M}} \quad (2)$$

Practically, implementation of a digital IIR filter of order N, requires a (2N+1) number of coefficients and multipliers with (1N) number of 2-input adders. In order to establish a general form by which designing IIR systems is truly implemented based on standard representation, famous realization forms are available. Therefore, realization of digital IR filters can be done through multiple methods.

In this paper, direct form II was chosen as the filter realization method for the implementation of the proposed IIR system. In direct form II, the arrangement of poles comes before zeros. Differently, the transfer function of direct form II originates from two transfer functions one is for zeros and the other is for poles as illustrated in equation (3) and (4) respectively [5].

$$H_1[Z] = \sum_{k=0}^{N-1} B_k Z^{-k} \quad (3)$$

$$H_2[Z] = \frac{1}{1 + \sum_{k=1}^{M} A_k Z^{-k}} \quad (4)$$

Where $H_1[Z]$ includes the zeros while $H_2[Z]$ includes the poles. Theoretically, cascading $H_2[Z]$ and $H_1[Z]$ in this order produces direct form II in which number of delay blocks is reduced which can strongly contributes in providing faster performance along with more economical property when compared to direct form I as one of other digital realization forms. Direct form II is also famous of the name canonic realization form in which each recursive and non-recursive signals can be obtained from a single delay element in order to verify the minimum number of delay elements. Figure 1 shows direct form II for a digital IIR filter. It is clearly shown from figure (1) that the delay unit is shared between input and output signals' path. Also, it obviously illustrated that the system is a recursive system since the feedback is taken back to take part in the system requirements.

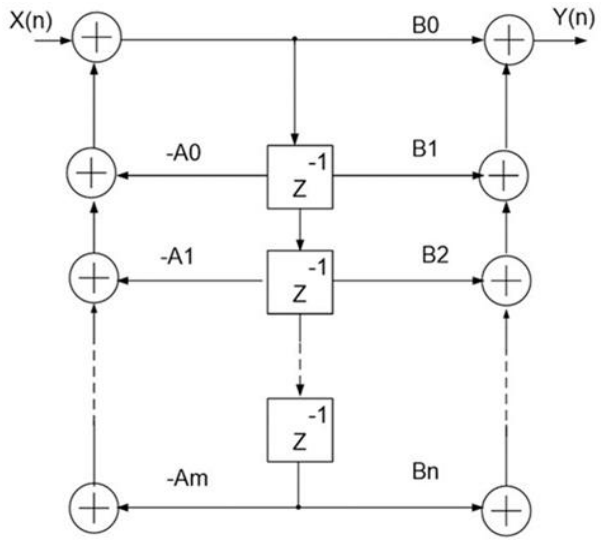

Figure 1. Realization digital IIR system using direct form II.

3. Design of proposed (IIR) filter circuit

In order to achieve realization of digital filters with the delay elements reduced to half as much as the case of the direct form I, direct form II has been regarded to be the implemented signal flow diagram. Due to the impracticality and instability of numerical evaluation for complicated filter designs, direct form I has been substituted by direct form II which is more practical and economical than direct form I. For a second order direct form II realization structure, the equations that describe its signal flow graph can be formulated as in Equation (5) and Equation (6) shown as follows:

$$v(n) = x(n) - a_1 v(n-1) - a_2 v(n-2) \quad (5)$$

$$y(n) = x(n) - b_1 v(n-1) + b_2 v(n-2) \quad (6)$$

Where v(n) and y(n) refer to the filter transfer function numerator and denominator respectively. Also, direct form II is called as a two-pole system that is followed in series by two-zero system which is different from the structure of direct form I. Therefore, the delay elements will be shared between the all-pole and all-zero sections which eventually adds a good property to the direct form II realization in terms of being faster and more economical than direct form I.

Regarding other realization forms of digital filters, it was preferred to have it as a future work since the focus of this research is mainly about designing the IIR filter based on the structure of direct form II. Due to that, D flip-flop (DFF) registers, adders and multipliers are required to build the suggested filter. The block circuit diagram of the IIR filter, in terms of logical representation is illustrated in Figure 2.

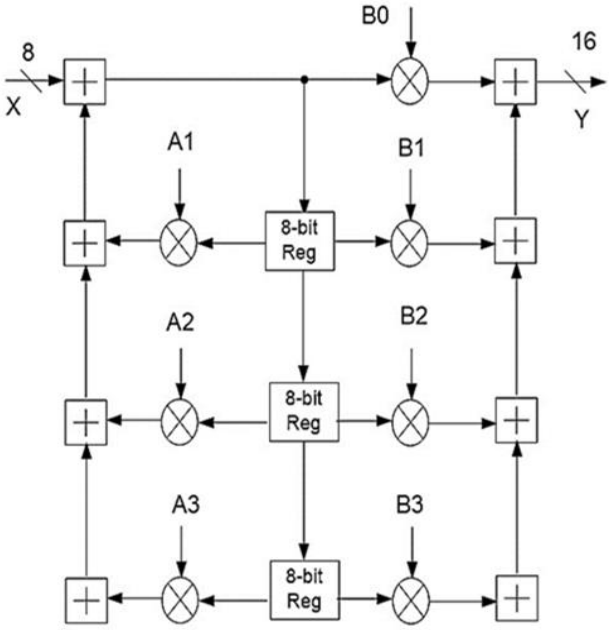

Figure 2. Block circuit diagram of the digital IIR filter.

4. Multiplier circuit design techniques

As shown in Figure 2, the IIR circuit diagram declares clearly that the design is constructed of registers, adders and multipliers. The multiplier is considered as the most important factor since it plays the major role in enhancing the performance of the proposed circuit.

In addition to the array multiplier, which comprises multi-layers of adder circuits regarding to the multiplier-bit inputs [28-30], various techniques and approaches of multiplier design have been applied in this paper in order to architect the suggested IIR filter so as to opt the best choice. Some of these techniques are listed below.

4.1 Mux-multiplier circuit design

Mux-multiplier is a new technique which was exploited to architect the 8-bit multiplier based on the multiplexer and multi-bit input adder, defined as Mux-multiplier. Figure 3 presents the circuit of Mux-multiplier. It is

shown that the idea of the design depends on setting a 2x1 multiplexer to feed the group of A data while grounding other input branches. On the other hand, data of group B are employed to be the controlling selectors for each single multiplexer in the design [31].

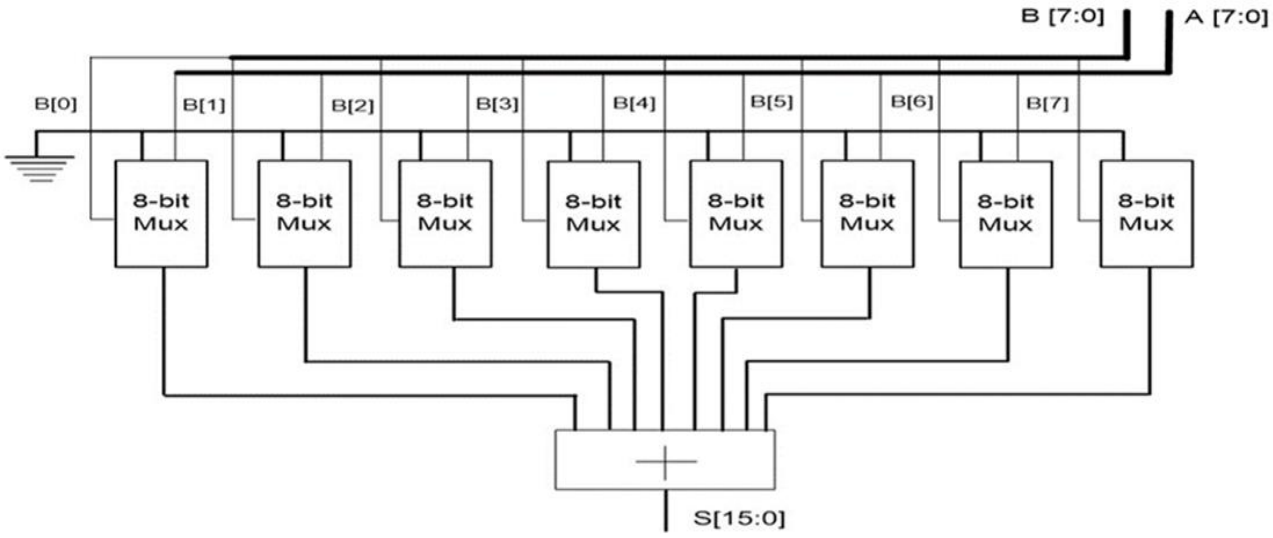

Figure 3. Mux-multiplier circuit

4.2 Parallel multiplier using two splitting circuit

This Multiplier is designed based on two margined circuits, defined as; the truncated and the least significant bit (LSB) circuits. The LSB circuit processes the lower four bits denoted as [3- 0] as in Figure 4. It consists two pairs of 2x4 multipliers with appropriate adders. The LSB multiplier circuit diagram is shown in Figure 4.

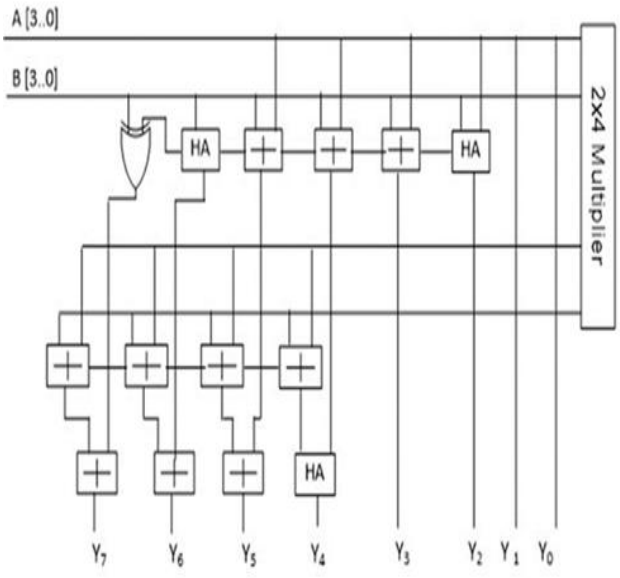

Figure 4. the least significant bit (LSB) multiplier circuit

The second circuit is the truncated multiplier. It is used to procedure the excessive 4 bits [7-4], as shown in Figure 5.

These circuits (Figures 4 and 5) are combined together in order to implement the Parallel Multiplier [32]. This technique is advantageous because both circuits are working simultaneously to achieve the output result.

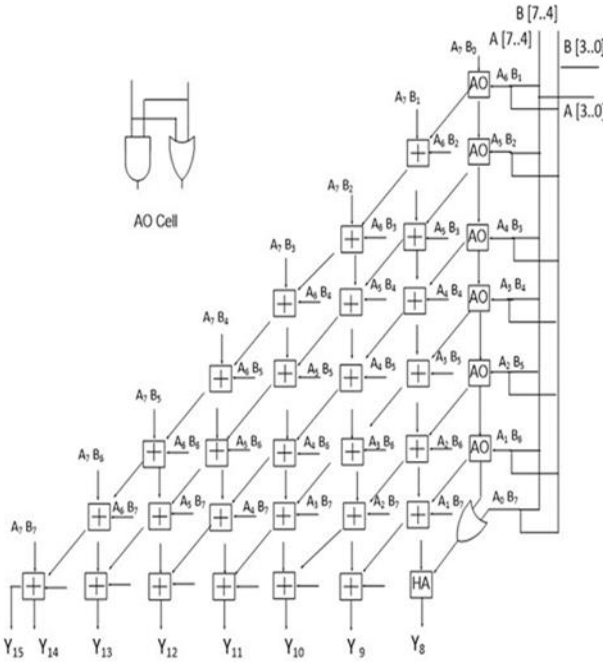

Figure 5. 4-bit truncated multiplier

4.3 Parallel multiplier using BCD decoder

The basic idea of this design is to use the binary coded decimal (BCD) decoder technique to prepare the 4x4 multiplier circuit [33]. Hence, and the achieved 4-bit circuit is used to implement the 8-bit multiplier. The interpretation of the idea is demonstrated in Figure 6.

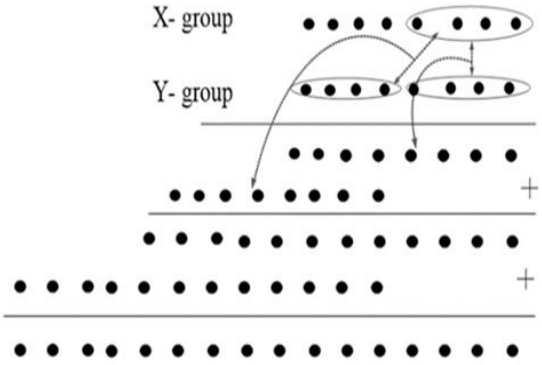

Figure 6. Multiplicand concept of the 8-bit BCD-multiplier

4.4 Multiplier based Vedic mathematics

A Vedic mathematics method is a popular approach. It is mostly exploited to architect the multiplier circuit in various techniques. Figure 7 (a) and (b) explains the multiplication idea for decimal and binary digit bit successively. The given 4-bit Vedic multiplier is used to accomplish the 8-bit multiplier [34].

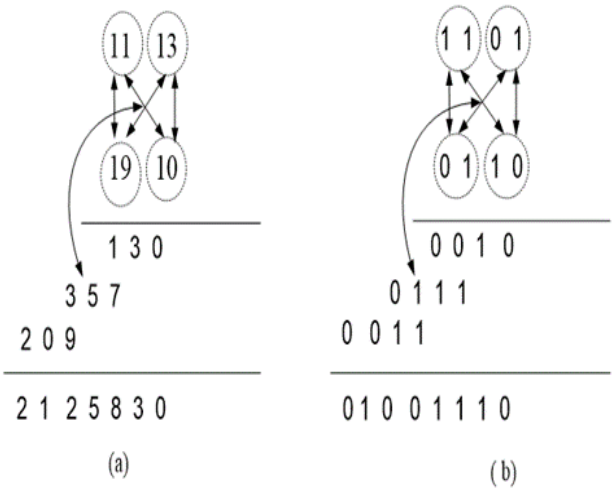

Figure 7. The Vedic mathematics concept: for (a) Decimal, and (b) Binary Number

5. Results and Discussions

To implement the IIR filter circuit on FPGA kit, programmed files ought to be coded using Quartus II software. Therefore, the consisted logic circuits applied to architect the proposed IIR filter design, have been coded in Verilog hardware description language (HDL) codes. The coded files are elaborated and synthesized using Quartus II and subdued to gate level simulation using ModelSim5.6 software to ensure the achieved results. The coded files of multipliers, adders, and registers are applied into the proposed IIR filter. The register transfer level of the designed IIR filter is shown in Figure 8.

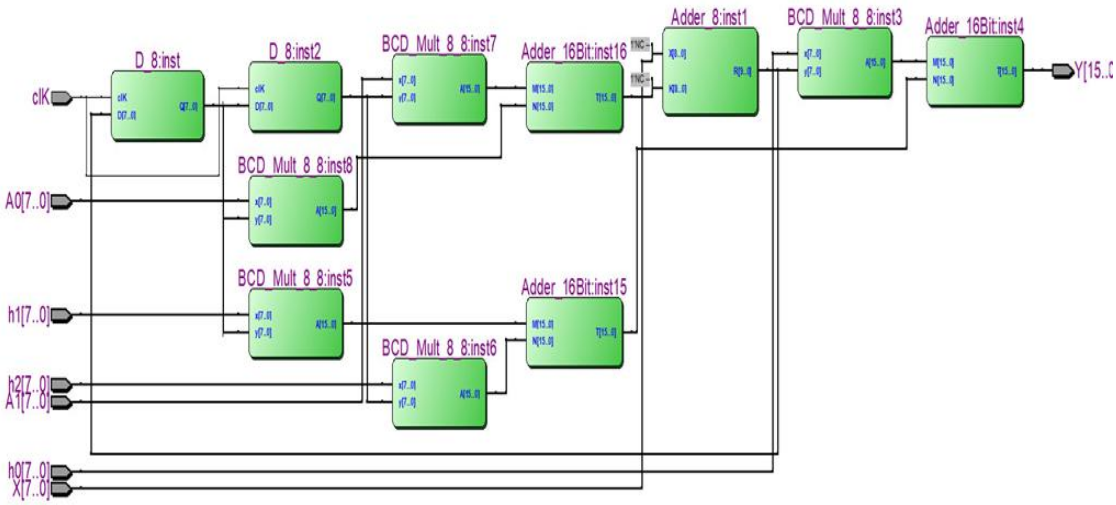

Figure 8. Register transfer level (RTL) viewer of the designed IIR filter

The Verilog HDL file of the proposed IIR filer circuit is used by the ModelSim5.6 software in order to investigate the validity of the circuit. The gate level simulation results have been done by implementing the programmed IIR filer code on the FPGA kit platform Cyclone IV GX type. The adopted results declare that the output values are identical to the mathematically calculated results. The gate level simulation of the proposed IIR filter has been executed through the preparation of the required testbench code while considering a time scale of 1ns/1ps. The specified simulation time is set as 1 second with a clocking period of 50 nS. The input values for h_0, h_1 and h_2 are set at 2, 3 and 4 respectively, while the X, A_0 and A_1 values are consistently varied in the sequence: (0, 2, 8 – 1, 2, 8 - 2, 2, 8 - 3, 2, 8 - and 4, 2, 8). The testbench code is configured with the mentioned values to ensure that the simulated results align with those obtained through mathematical computations. The gate level simulation results are shown in Figure 9.

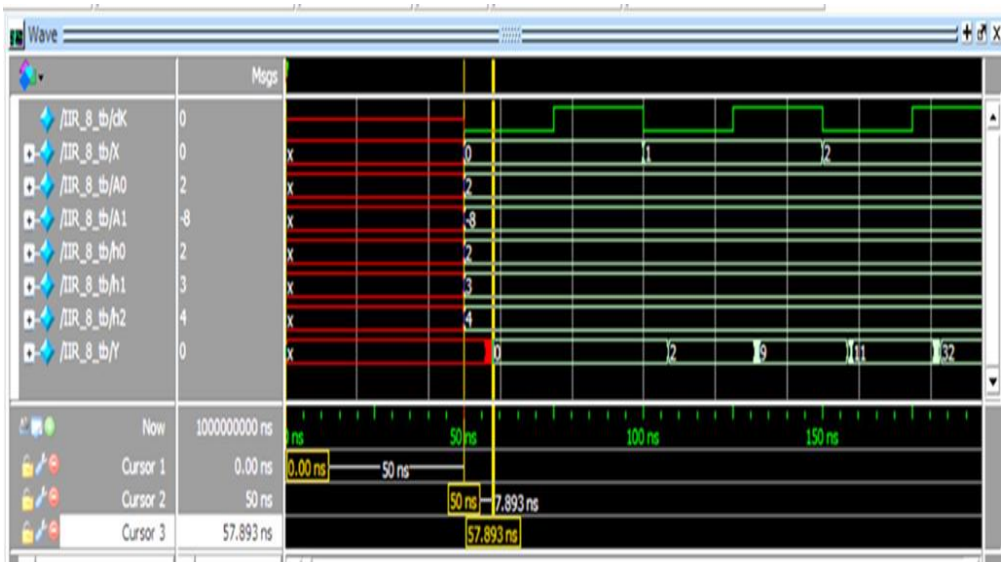

Figure 9. The gate level simulation results of the IIR filer

Figure 9 clarifies the input values X of the designed IIR filter, as well as $A_{[1,0]}$, $h_{[2,1,0]}$ and Y output. The achieved results are obtained through applying the BCD-Multiplier. The results illustrated in Figure 9 declare that the throughput output of the given circuit lasts 7.893 ŋSec in order to appear on the output and run with an operating speed of 282.8 MHz.

The BCD multiplier implementation on FPGA is established through preparing the required Verilog HDL files of the multipliers, adders and the DFF registers. The coding files are gathered into the proposed IIR filter. Then the process is evaluated through using the features of the Quartus II software by converting the Verilog HDL file into symbols. Then, converted files are all managed through using the schematic circuit diagram to architect the proposed IIR filter circuit. The successfully elaborated and synthesized IIR filter circuit converts it again to the Verilog HDL file in order to be programmed and implemented on the FPGA kit platform. Multiple types of designed multiplier circuit based on various techniques and methods have been used throughout this paper in order to specify the best multiplier circuit which can effectively put its positive impact on the performance of the proposed IIR filter. In addition to the conventional 8-bit array multiplier, another multiplier circuits are designed by the author such as: two margined circuit of Booth and parallel multiplier, Vedic multiplier based on Vedas mathematic, Mux-Multiplier that designed based on 2-1 multiplexer and the BCD-multiplier based on BCD decoder. The presented IIR filter has been operated on Quartus II and ModelSim 5.6 software. The power consumption has been calculated for each multiplier utilized in IIR filter circuit with the Cyclone IV GX FPGA kit. The

power-play power analyser indicates that BCD multiplier dissipates a total power of 88.32 mW, including 81. 23 mW of static power dissipation and 7. 09 mW of I/O thermal power dissipation. The results demonstrate the priority of the BCD multiplier over other multiplier types. The comparison results of the power consumption are listed in Table 1. Designing IIR filter is quite beneficial as it leads to enhancements of signal-to-noise ratio since it contributes in reduction of interferences of noisy and unwanted signal that may come from different sources.

Table 1 declares the values of multiple multipliers circuits which were applied to the IIR filter. A comparison results of the used multiplier is shown in Table 1.

Table 1: Multiple multipliers circuit applied to the IIR filter design

Multiplier	Technique	logic elements	Freq. operation (MHz)	Power Dissipation (mW)	Delay (ŋSec)
Array multiplier	Multi-layer adders	839	88.5	89.23	10.51
Parallel multiplier using two circuits	booth & parallel	828	121.05	89.13	10.39
Vedic multiplier	Vedic mathematics	661	131.2	88.37	9.38
Mux-multiplier	Approx. Multiplexing	686	78.24	89.23	10.71
BCD-multiplier	BCD decoding	188	282.8	88.32	7.89

A comparison is arranged based on number of logic elements, frequency operating speed, power dissipation and the delay time. Table 1 clearly declares the advantages of using the BCD-multiplier over other designs. It has the lowest number of logic elements (188), highest operation speed (282.8 MHz) and less delay time (7.89 ŋSec).

The comparison of the BCD multiplier was done only with presented multipliers including array multiplier, parallel, Vedic and Mux-Multiplier, using the same FPGA kit platform (Cyclone IV).

The comparison excludes some of other types such as Booth multiplier which gives non-accuracy approximated results (only the top half digit bits). The other multipliers may have advantages in the terms of speed operation, such: Wallace, and Carry-Save multipliers, but they look complex circuitry and require large area due to the tree structure (in case of Wallace multiplier), whereas the Synchronous, Dadda and Carry-Save multipliers drawbacks are the intricate to execute.

The achieved result of the proposed IIR filter based on BCD-multiplier compared to other works is illustrated in Table 2. The comparison is applied based on FPGA types, frequency operating speed, number of slices and the delay time.

Table 2: Comparison of the proposed IIR filter based on BCD-multiplier compared to the other works

Multiplier	Technique	Freq. operation (MHz)	Logic elements	Delay (ŋSec)
[35]	Virtex-5	32.63	854	38.02
[36]	NA	NA	1582	30.74
[37]	Zynq	53.51	1799	18.68
Proposed	Cyclone IV	282.8	188	7.89

Table 2 results declare the advantages of the proposed IIR filter over other works in the terms of frequency operating speed, number of slices and the delay.

Considering that this comparison is based on different FPGA kits such as Cyclone, Virtex and Zyng, it is due to the use of different software such as Quartus II, which uses Altera FPGA and ISE Xilinx FPGA family kits.

The IIR Lattice Filter based on floating point adder in [35] implemented on Virtex-5 FPGA

device using Xilinx 14.4 ISE. The obtained results are 32.63 MHz, 38.02 ŋSec for frequency operating speed and delay time.

In [36], the implementation of the second order IIR filter using the Vedic multiplier declares the path delay for the testing speed (30.74 ŋSec), and the number of slices (1582).

In [37], a second IIR Notch/anti-notch filter is implemented on a Xilinx ISE 14.4 Zynq FPGA series. The archived maximum frequency operation speed is 53.51 MHz, and the minimum period without Retiming has 29.2 ŋSec while with Retiming the delay time improves the minimum period to 18.686 ŋSec.

With respect to the previous considerations, the results obtained from the proposed IIR filter based on the BCD multiplier shows an advantage in the frequency operating speed, number of slices and the delay time compared to the aforementioned works.

6. Conclusions

Enhancement of the performance of digital IIR filter circuit architecture is increasingly important since these devices are greatly involved in many applications. However, paying attention to the multiplier design, which has the most powerful role in the IIR systems, was the main focus of this paper. Therefore, various multiplier circuits based on multiple architectures, such as array multiplier, Booth Parallel, Vedic, Mux-Multiplier and BCD-multiplier, were utilized to correctly choose the best among them for IIR system design depending on the best properties regarding to the logic elements, operation speed and delay time. Having been coded, synthesized, and gate level simulated using Verilog HDL code QuartusII 15, and Cyclone IV GX FPGA kit and ModelSim 5.6 respectively, the criteria of approving the best multiplier architecture was decided based on the performance of each individual multiplier circuit. The BCD multiplier has recorded the fewer number of logic elements of (188) with about a 71% lesser than the lowest logic elements of other compared approaches. Moreover, it recorded the higher frequency operation speed of (282.8 MHz) of about 53% faster than the fastest frequency operation of other approaches. Also, the BCD multiplier revealed the priority of having the minimum delay time of (7.89 ŋSec) of about 16% less than the lowest delay time of other designed approaches. Hence, it is clearly shown that the IIR filter designed based on BCD-multiplier architecture method has ranked among other IIR filters designed based on other multiplier techniques. To sum up, looking forward to develop the multiplier features will considerably contribute in the enhancement of any system on which the multiplier is mainly involved in its design.

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