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Analyzing the Influence of SiO_2 Buried Layer Thickness and Positioning on the Performance of 20 nm N-MOSFETs

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ABSTRACT

The continuous scaling of MOSFETs to meet the demands of high-performance devices has intensified challenges such as short-channel effects (SCEs), which degrade device reliability and efficiency. To address these issues, this study investigates the influence of SiO_2 buried layer thickness and vertical positioning on the electrical performance of 20 nm n-MOSFETs incorporating a high-k dielectric gate stack. Using TCAD Silvaco ATLAS, the research systematically evaluates how buried oxide thickness (10 nm to 50 nm) and depth (30 nm to direct contact with the channel) affect key device parameters, including threshold voltage (V_{th}), drain-induced barrier lowering (DIBL), breakdown voltage, ON current (I_{on}), leakage current (I_{off}), and the I_{on}/I_{off} ratio. Results show that increasing the buried layer thickness increases I_{off} from 8.51×10^{-11} A/m (without buried layer) to 3.09×10^{-10} A/m at 50 nm, while I_{on} slightly increases to 2.3×10^{-3} A/m. Although this reduces the I_{on}/I_{off} ratio from 2.37×10^{7} to 7.54×10^{6}, it also significantly improves breakdown voltage from 85.09 V to 167.4 V at 10 nm thickness. Notably, the breakdown voltage decreases to 76.26 V at 50 nm. In terms of vertical positioning, placing a 10 nm SiO_2 buried layer in direct contact with the channel yields the highest breakdown voltage of 1186.7 V and the lowest I_{off} of 5.15×10^{-11} A/m, with an I_{on}/I_{off} ratio of 3.62×10^{7}. These results highlight that both the thickness and position of the buried oxide layer play a crucial role in suppressing SCEs and enhancing breakdown robustness.

1. Introduction

The progression of fabrication techniques with each generation of semiconductor devices yields smaller, quicker, and lower-power integrated circuits [1]. The miniaturization of conventional MOSFET devices creates short-channel effects (SCEs), leading to a reduction in device performance. The I_{on}/I_{off} ratio, breakdown voltage, threshold voltage (V_{th}), and drain-induced barrier lowering (DIBL) are characteristics significantly influenced by the scaling process. To further scale, novel device architectures are necessary to enhance performance in the nanoscale domain for the next generation of devices [2-4]. Gate engineering is an important technique for solving negative impacts such as DIBL, gate leakage current, and SCEs. This approach encompasses such double gate, tri-gate, FinFET, and gate all-around (GAA) structures, providing a different approach for simultaneous suppression of SCEs, and enhancement of device performance by reducing leakage and tunnelling currents, achieved through meticulous control of the gate material workfunction [5,6]. Using high-k as a gate material for scaled-down devices enhanced current performance. The employment of high-k materials as gate dielectrics offers the benefits

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of diminished parasitic capacitances and lower off-current. Owing to the benefits provided by high-k materials, HfO_2 is employed as a dielectric of the gate in the MOSFET structure [7]. A possible solution to the challenges of MOSFET scaling is to incorporate a buried layer. The addition of a buried oxide layer (BOX) enhances the characterization of the MOSFET, hence improving the device's performance. This technology is referred to as a Silicon-on-Insulator Metal-Oxide-Semiconductor Field-Effect Transistor or SOI-MOSFET. SCEs in SOI-MOSFETs are significantly mitigated, as demonstrated both theoretically and practically by numerous researchers [8]. The advantages of SOI mostly arise from its reliance on film thickness, as well as body and back gate (the substrate) biases. This reliance facilitates enhanced regulation of drain bias, carrier velocity saturation, channel length modulation, and its impact on output conductance, and device deterioration attributed to channel effect immunity in SOI-MOSFETs. The implementation of SOI-MOSFETs in VLSI circuits offers designers more flexibility than bulk-MOSFET designs [9,10]. Nano MOSFETs may be utilized in several applications, including embedded PCB systems to enhance hybrid system control [11, 12], the construction of embedded ICs for high-frequency communications systems [13], and control systems for operated vehicles in underwater applications [14].

Since 2014, a comparison study utilizing Silvaco ATHENA and ATLAS has shown that the presence of buried oxide in 45nm MOSFETs reduces the charge between the drain and source, and increases the ON current (I_{on}) when compared to 45nm conventional bulk MOSFETs [15]. One year later, the SiO_2 buried layer thicknesses of 100 nm, 50 nm, and 10 nm were analysed using the ATHENA and ATLAS modules to investigate the behaviour of MOSFETs. The electrical characteristics of 100 nm thickness are marginally superior compared to those of 50 nm and 10 nm. At thicknesses of 10 nm and 100 nm, the I_{on} current was seen to decrease by 6.9% and 11%, respectively, in comparison to a thickness of 50 nm. Consequently, the 50 nm thickness aligns more closely with the ITRS 2013 series prediction [16]. Anvarifard et al. [17] produced a nanoscale SOI-MOSFET in Silvaco ATLAS with a redesigned channel at the drain side, which reduces the electrostatic coupling between the drain and the channel. SCEs are reduced by the presence of the BOX layer in the substrate. Priya et al. [18] utilized Silvaco ATLAS to build a 60 nm channel length triple metal gate MOSFET, using varying thicknesses of the oxide buried layer from 10 nm to 50 nm. Compared with the other thicknesses, an optimal BOX thickness of 50 nm was demonstrated at a channel length of 60 nm, yielding a large I_{on} and a low I_{off}, resulting in an I_{on}/I_{off} ratio of around 10^9. The minimum channel length is affected by the work function of the gate, as demonstrated in a study by Su, Elizabeth Mei-hua, et al. [19], which indicates that while the BOX thickness has a minor impact on the minimum channel length of MOSFETs, the channel thickness has a significant effect. They studied the behaviour of MOSFET, with channel length ranges from 10 nm to 200 nm, implanted by a buried oxide layer, SiO_2, with thickness ranges from 10 nm to 200 nm. The results indicate that the minimum channel length of a MOSFET is marginally influenced by the thickness of the buried oxide layer, although it is significantly impacted by the channel thickness. The minimum channel length is influenced by the work function of the gate. Bhuyan et al. [20] employed Silvaco ATHENA and ran simulations using ATLAS to build a BULK n-MOSFET featuring a 100 nm channel in 2022, then compared its electrical attributes with other multi-gate engineering designs. The results demonstrated that the multiple gate design is more dependable and economical, exhibiting substantially reduced power dissipation and consumption. The breakdown voltage is a key parameter in aerospace and military applications, encompassing microwave devices, communication circuits, and optical technologies. In 2023, Pu et al. [21] employed TCAD to investigate the enhancement of breakdown voltage in SOI-MOSFETs beneath the gate electrode to avoid penetration from the gate to the channel. The adjustments improved the device's breakdown voltage by dispersing

the electric field and charge density away from the critical areas next to the gate electrode. The suggested composite device increases the breakdown voltage by around 79%. The breakdown voltage of this device was 17 V, while the breakdown voltage of its ordinary counterpart is roughly 9.5 V. Tayade et al. [22] examined the design of a 100 nm MOSFET with HfO_2 gate dielectric to mitigate gate tunnelling, with the channel supplied by two different materials, separate silicon and graphene formulas. Upon comparison, it was determined that both exhibited favourable outcomes; however, graphene demonstrated enhancements in the DIBL and sub-threshold slope (SS) metrics. In the investigation of SCEs in MOSFET, the device was miniaturized to 20 nm length with two different materials used for channel, for a 20 nm graphene channel, enhancements in I_{on} and SS, making it appropriate for low power and high-speed applications.

While considerable advancements have been made in SOI-MOSFET technologies, a critical research gap persists regarding the combined influence of BOX thickness and its vertical positioning relative to the channel, particularly in 20 nm scaled devices. Previous studies (e.g., Aziz, MNIA., et al. [15]) primarily focused on optimizing the channel length with fixed BOX configurations, while others (e.g., Aziz, M. N. I. A., et al. [16] and Priya et al. [18]) investigated BOX thickness or gate structure variations independently, showing improvements in I_{on}/I_{off}. However, these works did not explore systematic changes in BOX placement. Moreover, although Pu et al. [21] reported enhanced breakdown voltage, it did not examine how BOX geometry might contribute to this improvement. Tayade et al. [22], while investigating material innovations such as graphene channels and HfO_2 dielectrics, did not consider structural BOX modifications. This study fills that gap by systematically analyzing how simultaneous variations in BOX thickness and proximity to the channel affect key device metrics I_{on}, I_{off}, I_{on}/I_{off} ratio, and breakdown voltage in SOI-MOSFETs with advanced high-k gate dielectrics. Our work advances the field by offering new insights into BOX engineering as a practical design knob for performance optimization in nanoscale devices.

In this work, the performance of the 20 nm MOSFET has been evaluated by examining its electric field distribution, the V_{th}, and the breakdown voltage for varying SiO_2 buried layer thicknesses and positions. Additionally, the study includes an assessment of SCEs by analysing the DIBL and subthreshold slope characteristics to verify their resistance to short-channel issues. These parameters, along with the ON-to-OFF current ratio, were incorporated into the figure of merit (FOM) to assess the performance of each structure.

2. Methodology

Silvaco TCAD was employed for comprehensive simulations to analyse the characteristics and performance of the MOSFET device [23]. The simulation involved the design of the n-MOSFET structure with a 20 nm channel length. Table 1 illustrates the main parameters used in the structural design of the n-MOSFET.

Table 1: Parameters of designing 20nm n-MOSFET.

Parameters	value
Channel	20nm Si
Doping of Source and Drain	$5 \times 10^{20}\ cm^{-3}$
Doping of the Channel	$9 \times 10^{17}\ cm^{-3}$
Doping of Substrate	$1 \times 10^{14}\ cm^{-3}$
Gate Work-function	4.55eV
Gate length	25nm
Source and Drain Length	40nm
Gate Dielectric Thickness	10nm
Silicon Film Thickness	15 nm

In this simulation framework, precise model selection is crucial. The models employed in this work include the Auger model for direct transitions involving three carriers, the SRH model for carrier-fixed minority lifetimes.

In this study, the Arora mobility model was employed within Silvaco ATLAS due to its proven reliability in modeling doping- and temperature-dependent carrier mobility in simulated device. This model is particularly suitable for nanoscale MOSFETs, as it captures

phonon and charge scattering mechanisms, which significantly impact carrier transport at high doping levels and reduced dimensions. In addition, standard models available in ATLAS such as Shockley–Read–Hall (SRH) recombination, and Auger recombination were included to ensure accurate modeling of recombination-generation and band structure modifications in the active regions. The numerical solution method, Newton-Gummel with trap autonr, is a parameter used to enable or control automatic non-radiative recombination through traps in a semiconductor simulation. It helps simulate Shockley-Read-Hall (SRH) recombination more accurately by allowing ATLAS to dynamically model how traps behave under different biasing and carrier injection conditions. Newton-Gummel with trap autonr combination is especially important in nanoscale MOSFETs, where interface traps and bulk defects can significantly influence leakage current, subthreshold slope, and threshold voltage behaviour [24]. HfO_2 is classified as a high-K dielectric utilized as a gate dielectric to diminish gate tunnelling leakage, hence enhancing the performance of MOSFETs [25]. Hence, the MOSFET is scaled down from a 100 nm channel to a 20 nm channel length, with HfO_2 gate dielectric [22]. The use of a buried layer may influence the performance of the MOSFET [26]; therefore, we investigate the device characteristics by employing a buried layer in a 20 nm channel length MOSFET, as shown in the structure view of Figure 1. This study is categorized into two parts, focusing on a comparative analysis of the effects of the thickness and position of the buried layer on MOSFET performance.

This part of the current study examines the incorporation of SiO_2 buried layer in MOSFET. A buried layer is located at 30 nm below the active channel region, possessing an initial 10 nm thickness. The thickness of the buried layer grows gradually as it approaches the substrate to examine its impact on device performance. The increment of the buried layer occurs in a 10 nm step, ending at 50 nm thickness. The variable thickness of the buried SiO_2 layer is anticipated to affect critical aspects of the MOSFET's performance. A comprehensive comparative analysis is performed to assess the main performance parameters under two distinct configurations: one representing the MOSFET without a buried layer and the other incorporating the graded thickness of the buried layer. The research aims to optimize the buried layer design to enhance electrical performance and reliability in advanced semiconductor devices. This method emphasizes the importance of engineering buried layers in the miniaturization of MOSFETs for future applications.

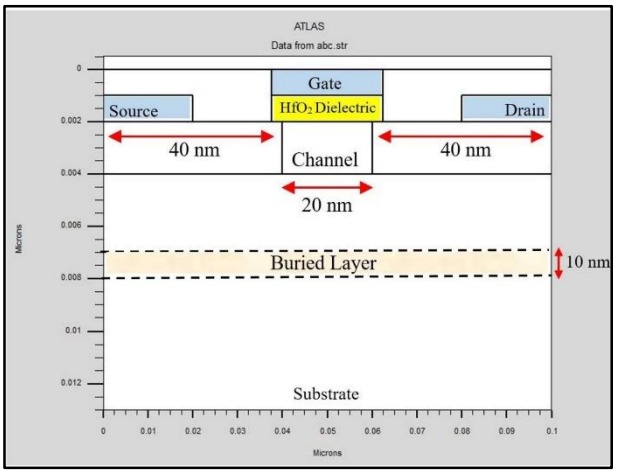

Figure 1. Schematic view of 20nm channel MOSFET with 10 nm SiO_2 thickness buried layer.

Part two discusses the ideal thickness of the SiO_2 buried layer is originally established based on the results acquired from the previous simulation in part one. This thickness indicates the most effective design for supplying the necessary performance metrics in the construction. Upon identification, the buried layer is shifted up for direct contact with the channel region, facilitating a more accurate assessment of its impact on the MOSFET's behaviour. This study conducts a comparative evaluation to examine the impact of varying buried layer thickness on the performance of the current stage. This study is fundamentally dependent on the basic parameters set during the prior simulation section, ensuring continuity and uniformity between the steps. To accomplish this, the buried layer is shifted up in four various configurations, each illustrating a unique thickness scenario. This incremental technique attempts to comprehensively examine

the influence of the buried layer's thickness and its position variations on the MOSFET's characteristics. These alterations provide a greater understanding between the buried layer and the device, yielding critical insights for optimizing the structural design to improve device performance.

3. Results and Discussion

3.1 SiO_2 buried layer thickness variation

Figure 2 depicts drain current (I_d) versus gate voltage (V_g) characteristics for two different designs of MOSFET configurations. The configurations are the conventional MOSFET structure without a buried layer and the MOSFET with a SiO_2 buried layer for different thicknesses varied from 10 nm to 50 nm with a 10 nm step. The buried layer was located along the source, gate, and drain at a depth of 50 nm from the gate-insulator interface. The placement of the buried layer is defined by its thickness, where thinner buried layers are closer to the channel, and thicker buried layers are farther from the channel. At first glance, the curves in Figure 2 reveal that the existence of the buried layer at different locations does not affect the trend of the MOSFET characteristics curve.

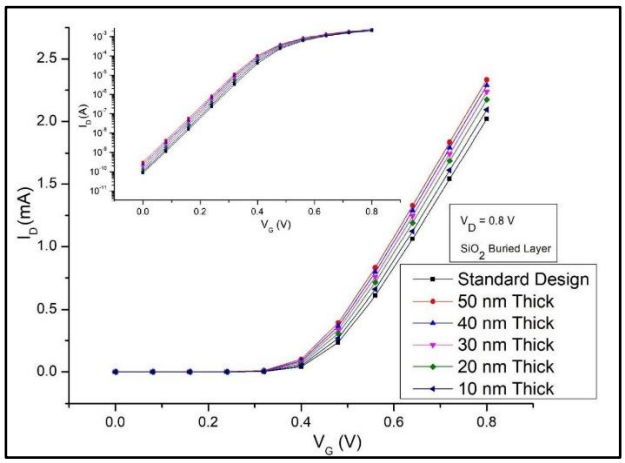

Figure 2. I-V Characteristics of 20 nm channel length MOSFET without buried layer (standard design) and the MOSFET with different thicknesses of SiO_2 buried layer.

It can be seen that for the conventional MOSFET curve, the drain current increases steadily with the applied drain voltage. This curve exhibits a smaller maximum drain current compared to the MOSFETs with a buried layer. It can be noticed a slightly reduced slope in the linear region (low V_g values) could indicate higher series resistance or limited mobility in the channel [27, 28]. The curves for MOSFETs with buried layers demonstrate an improvement in the drain current as the buried layer thickness is varied. For all buried-layer thicknesses, the I_d is higher at the same V_g compared to the conventional MOSFET. As the buried layer increases in thickness, the I_d is developed, and this could be due to improved channel conductivity or increased gate control effectiveness over the inversion layer [26]. The sub-figure in Figure 2 demonstrates that the introduction of the buried SiO_2 layer produces a small increase in the leakage current. The buried layer could cause an increase in the fringing electric fields and enhanced band bending at the interface of the buried layer and the substrate [29, 30].

Table 2 provides a detailed comparison of MOSFET performance parameters without a buried SiO_2 layer and with buried SiO_2 layers of varying thicknesses (10 nm, 20 nm, 30 nm, 40 nm, and 50 nm). Each parameter highlights how the presence and thickness of the buried layer affect the device's characteristics. It can be noticed that the V_{th} decreases with increasing SiO_2 thickness. Without the buried layer, V_{th} is 0.462 V, and for the thickest buried layer (50 nm), V_{th} reduces to 0.43 V. The SiO_2 buried layer reduces the substrate coupling, altering the electrostatics in the channel and lowering V_{th} [31]. It is also shown in Table 2 that the drain current when the MOSFET is fully turned on, I_{on} slightly increases with the buried layer's thickness, whereas without the buried layer, I_{on} is 2.0×10^{-3} A/m, and for the 50 nm buried layer, I_{on} increases to 2.3×10^{-3} A/m. This indicates that the existence of the buried layer improves gate control over the channel, enhancing inversion charge density and marginally increasing it. On the other hand, Table 2 reveals that the I_{off} increases significantly with the thickness of the buried layer, where without the buried layer, I_{off} is 8.51×10^{-11} A/m, and for the 50 nm buried layer, I_{off} rises to 30.9×10^{-11} A/m. The increase in the leakage current could be due

to the buried layer creating leakage paths due to fringing electric fields and tunnelling effects [32], leading to higher I_{off}. Deterioration caused by the presence of the buried layer on both I_{on} and I_{off} was reflected clearly in the I_{on}/I_{off} ratio, which is the indicating the device's ability to switch effectively between states, where the ratio decreases as the buried layer thickness increases. Without the buried layer, the ratio is 2.37×10^{7}, and for the 50 nm buried layer, the ratio drops to 7.54×10^{6}. The increase in I_{off} dominates the modest rise in I_{on}, degrading the switching performance.

Table 2: Main parameters of MOSFET with a 20nm channel length (A) without buried layer (B) with 10 nm (C) 20 nm (D) 30 nm (E) 40 nm (F) 50 nm thickness SiO_2 buried layer.

Parameters	A	B	C	D	E	F
	Without the buried layer	**10nm thickness SiO_2 buried layer**	**20nm thickness SiO_2 buried layer**	**30nm thickness SiO_2 buried layer**	**40nm thickness SiO_2 buried layer**	**50nm thickness SiO_2 buried layer**
V_{th} (V)	0.462	0.454	0.446	0.440	0.435	0.43
I_{on} (A/m)	2×10^{-3}	2.09×10^{-3}	2.1×10^{-3}	2.2×10^{-3}	2.28×10^{-3}	2.3×10^{-3}
I_{off} (A/m)	8.51×10^{-11}	1.01×10^{-10}	1.363×10^{-10}	1.8×10^{-10}	2.3×10^{-10}	3.09×10^{-10}
I_{on}/I_{off}	2.37×10^{7}	2.0×10^{7}	1.5×10^{7}	1.23×10^{7}	9.65×10^{6}	7.542×10^{6}
Breakdown Voltage (V)	85.09	167.4	124.46	102	86.9	76.266
DIBL (V/V)	0.3089	0.307	0.309	0.311	0.314	0.317

Although the SiO_2 buried layer dropped the main MOSFET performance parameters, Table 2 reveals that the breakdown voltage initially increases with increasing thickness of the buried layer up to 40 nm, then decreases for a thickness of 50 nm. The breakdown voltage without the buried layer is 85.09 V, and it increases as the thickness grows from 10 nm to 40 nm, peaking at 167.4 V for 10 nm. For 50 nm, the breakdown voltage drops to 76.27 V, even lower than the case without the buried layer. The introduction of the SiO_2 buried layer improves the breakdown voltage initially because the buried layer adds an insulating barrier that suppresses the vertical electric field in the bulk substrate [33]. This reduces charge injection from the substrate and improves isolation between the drain and source regions. Thicker buried layers (up to 40 nm) enhance this effect, providing a stronger barrier to charge transport and delaying the onset of avalanche breakdown. When the buried layer thickness reaches 50 nm, the breakdown voltage decreases significantly. This can be explained as a thicker buried layer enhances fringing fields near the edges of the MOSFET, especially at the drain junction. These fringing fields locally concentrate the electric field, accelerating the breakdown process and lowering the breakdown voltage. Also, a thick buried layer might introduce significant discontinuities in the substrate electrostatics, reducing dielectric strength. Increased parasitic capacitance and field crowding near the junctions further degrade the breakdown characteristics [34]. Finally, Table 2 shows that the existence of a buried layer has slight effect on the DIBL value, where its value is around 0.3 V.

Figures of Merit (FOM) [35] in Table 3 depict the optimum case between standard MOSFET (without buried layer) and different thicknesses of SiO_2 buried layer (10 nm - 50 nm). Employing the main parameters in the FOM equation, the parameters that need to be raised are placed in the numerator, and the parameters that need to be down are placed in the denominator, as shown in Equation 1. The FOM value of the standard MOSFET is 140.6 $\times10^{8}$. The FOM value of 10 nm thickness of the buried layer is raised to 249.9 $\times10^{8}$. It was noticed that FOM values decreased with increasing thickness of the buried layer even though the 50 nm thickness FOM value was 41.66 $\times10^{8}$. By observing the FOM table, the 10 nm thickness buried layer has a higher value, which indicates it is an optimum value.

Table 3: FOM of parameters in the bulk of MOSFET with a 20nm channel length (A) without buried layer (B) with 10 nm (C) 20 nm (D) 30 nm (E) 40 nm (F) 50 nm thickness SiO_2 buried layer.

	A	**B**	**C**	**D**	**E**	**F**
	Without the buried layer	**10nm thickness SiO_2 buried layer**	**20nm thickness SiO_2 buried layer**	**30nm thickness SiO_2 buried layer**	**40nm thickness SiO_2 buried layer**	**50nm thickness SiO_2 buried layer**
FOM	140.6×10^8	249.9×10^8	139.7×10^8	91.2×10^8	63.08×10^8	41.66×10^8

$$\text{FOM} = \frac{I_{on} \times BV}{I_{off} \times V_{th} \times DIBL} \quad \ldots (1)$$

Figure 3 illustrates the electric field distribution in the bulk of a 20 nm MOSFET simulated using Silvaco ATLAS. The electric field plots are shown for Figure (A), a conventional MOSFET without a buried layer, and Figures (B) to (F), MOSFETs with a SiO_2 buried layer, where the thickness of the buried layer increases from 10 nm (Figure B) to 50 nm (Figure F). Figure 3A shows that the electric field lines are more evenly distributed in the substrate. The maximum electric field is concentrated near the source and the drain junction and decreases as we move toward the bulk substrate. By inserting a SiO_2 buried layer, a significant alteration in the electric field distribution was obtained [36]. As the buried layer thickness varies from 10 nm to 40 nm, the field is redirected and confined closer to the drain and the buried layer, particularly above the SiO_2 layer. For a 40 nm buried layer, the suppression of the field in the bulk is most effective, but poor-quality buried oxides, such as the introduction of interface states that can distort the field distribution and impact device reliability [37]. At a 50 nm thick buried layer, the electric field distribution near the drain (right side) shows increased fringing effects at the edges of the buried layer. The electric field becomes more concentrated near the drain junction, with less uniformity compared to the 40 nm case, moderate buried layer thicknesses in the 20-40 nm range appear to provide an optimal trade-off between improved electrostatic control and minimal parasitic effects [38]. When the buried layer becomes too thick, the fringing electric fields at its boundaries become significant. These fringing fields locally enhance the electric field intensity near the drain junction, leading to premature breakdown and increased substrate leakage due to localized field enhancements [30].

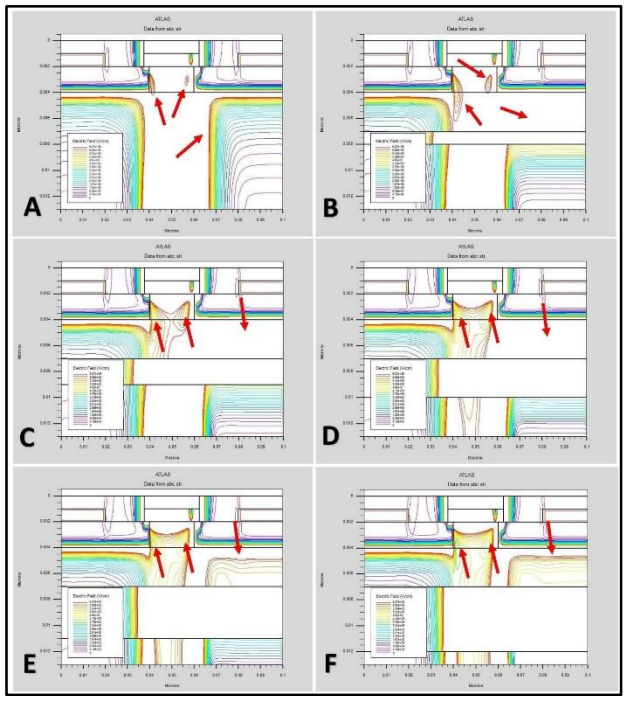

Figure 3. Electric field distribution in the bulk of MOSFET with a 20nm channel length (A) without buried layer (B) with (10 nm (C) 20 nm (D) 30 nm (E) 40 nm (F) 50 nm) thicknesses SiO_2 buried layer.

In terms of electric field distribution along the MOSFET channel, Figure 4 illustrates the electric field distribution along the channel of a 20 nm MOSFET for various cases of conventional MOSFET (i.e., without a buried layer), and MOSFETs with SiO_2 buried layers of different thicknesses ranging from 10 nm to 50 nm. It can be noticed that the behaviour of the electric field without and with the buried layer reveals a field peak sharply at the source end of

the channel due to the injection of carriers from the source. Along the channel, the electric field reduces but remains relatively high across the middle portion. At the drain end, another peak is observed, resulting from high-field regions near the drain. The buried layer reduces the electric field intensity in critical regions (source and drain), which improves reliability by minimizing hot carrier effects and lowering the risk of breakdown.

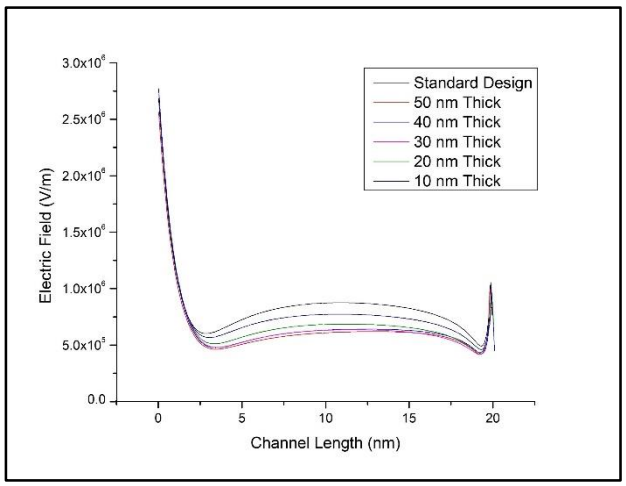

Figure 4. Electric field distribution along the channel of MOSFET with a 20nm channel length without buried layer (standard design) and with different thicknesses of SiO_2 buried layer.

3.2 SiO_2 buried layer position variation

Figure 5 depicts the characteristics of four distinct MOSFET designs, illustrating the relation between the I_d and the V_g. The comparative study investigated the effects of shifting up the position of a 10 nm thickness of SiO_2 buried layer, even if it reached beneath the channel. The buried layer was embedded in the substrate adjacent to the MOSFET at a depth of 30 nm below the channel. The position of the buried layer is changed at different locations, which could raise the potential enhancements in MOSFET performance. The device with a 10 nm thick buried layer is chosen due to demonstrated optimal results compared to other thicknesses in prior simulations.

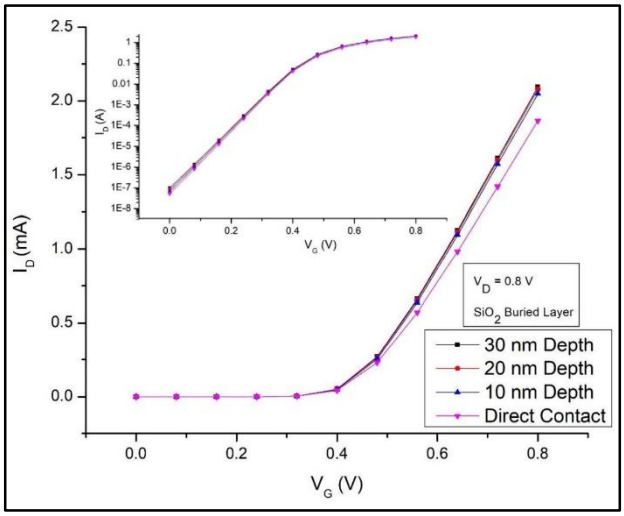

Figure 5. I-V Characteristics of 20 nm MOSFET with 10 nm SiO_2 buried layer at depth (30 nm, 20 nm, 10 nm, and direct contact with the channel).

The curves in Figure 5 demonstrate that the trend of the MOSFET characteristics curve is somewhat altered by the implementation of the 10 nm buried layer at various places.

The MOSFET curve exhibits a continuous modest drop in drain current with increasing gate voltage, the minimal variation in the drain current for different positions of the 10 nm buried oxide layer suggests a limited electrostatic impact at such ultra-thin thicknesses. This outcome indicates that the influence of the buried layer becomes less significant when its thickness is reduced to the nanometre scale, where the field confinement effect is weak. A slight decrease in the slope of the linear region (low V_g values) is evident, possibly signifying heightened series resistance or limited charge mobility within the channel. It can also be seen in Figure 5 that the I_d-V_g curve of the MOSFETs with a 10 nm thick buried layer reveals a small reduction in drain current when the position of the buried layer is shifted upward from a depth of 30 nm to 20 nm. This shift brings the 10 nm buried layer into direct contact with the channel, leading to a modest decrease in I_d at the same V_g. This reduction can likely be attributed to reduced channel conductivity or diminished gate control efficiency over the inversion layer. The sub-figure in Figure 5 demonstrates that the elevated 10 nm thickness buried layer led to a significant decrease in leakage current. The thinner buried

layer may result in a decrease in fringing fields and reduced band bending at the interface between the buried layer and the substrate.

Table 4 presents a comprehensive comparison of MOSFET performance metrics of 10 nm SiO_2 buried layers of different positions at depths of (30 nm, 20nm, 10 nm, and direct contact with the channel). Each parameter illustrates the impact of the buried layer's presence and position on the device's characteristics. The elevation of the SiO_2 buried layer from a depth of 30 nm to 10 nm results in a nearly constant V_{th} of around 0.454 V.

The V_{th} increases somewhat to 0.464 V when the buried layer is in direct contact with the channel. The 10 nm SiO_2 buried layer, being in direct contact with the channel, enhances substrate coupling, modifies the electrostatics within the channel, and elevates V_{th}.

Table 4: Main parameters of 20 nm MOSFET with 10 nm SiO_2 buried layer at depth (30 nm, 20 nm, 10 nm, and direct contact with the channel).

Parameters	30 nm Depth	20 nm Depth	10 nm Depth	Direct Contact
V_{th} (V)	0.454	0.455	0.456	0.464
I_{on} (A/m)	2.09×10^{-3}	2.07×10^{-3}	2.04×10^{-3}	1.86×10^{-3}
I_{off} (A/m)	1.01×10^{-10}	8.57×10^{-11}	6.90×10^{-11}	5.15×10^{-11}
I_{on}/I_{off}	2.05×10^{7}	2.42×10^{7}	2.96×10^{7}	3.62×10^{7}
Breakdown Voltage (V)	167.4	262.3	494.9	1186.7
DIBL (V/V)	0.307	0.305	0.303	0.307

Table 4 indicates that the I_{on} when the MOSFET is fully activated, exhibits a slight decrease as the depth of the 10 nm buried layer varies from 30 nm to 10 nm. Specifically, at a depth of 30 nm, the I_{on} value is 2.09×10^{-3} A/m, while in the buried layer in direct contact with the channel, the I_{on} decreases to 1.86×10^{-3} A/m. It indicates that the presence of the buried layer impairs gate control over the channel, diminishes the inversion charge density, and slightly reduces it. Conversely, Table 4 indicates that the I_{off} diminishes significantly as the buried layer is shifted up; specifically, at a depth of 30 nm, the I_{off} value is 1.01×10^{-10} A/m, while direct contact between the buried layer and the channel results in a reduction of I_{off} to 5.15×10^{-11} A/m. The reduction in I_{off} may be attributed to the buried layer that blocks leakage pathways from the source/drain regions to the substrate; it could be due to the fringing field's reduction and tunnelling processes, resulting in a decrease in I_{off}. The enhancement resulting from the existence of the buried layer I_{off} was distinctly evident in the I_{on}/I_{off} ratio, which signifies the device's capacity to transition successfully between ON and OFF states, with the ratio increasing as the 10 nm thick buried layer is shifted up. At a depth of 30 nm, the ratio is 2.05×10^{7}, but for direct contact, the ratio increases to 3.62×10^{7}. The reduction in I_{off} predominates over the small decrease in I_{on}, resulting in enhanced switching performance. While the SiO_2 buried layer affected the performance of the main MOSFET characteristics, Table 4 indicates that the breakdown voltage initially increases as the 10 nm thickness of the buried layer is shifted up from a 30 nm depth to direct contact with the channel location. The breakdown voltage for a buried layer at a depth of 30 nm is 167.4 V, which increases significantly to 1186.7 V when the buried layer directly contacts the channel position. The incorporation of the SiO_2 buried layer enhances the breakdown voltage initially by providing an insulating barrier that mitigates the vertical electric field within the bulk substrate. This mitigates charge injection from the substrate and enhances isolation between the drain and source areas. Thinner buried layers enhance this effect, creating a more robust barrier to charge transmission and delaying the initiation of avalanche breakdown. When the 10 nm buried layer is shifted to direct contact with

the channel, the breakdown voltage dramatically increases compared to a 10 nm thickness at a depth of 30 nm. Ultimately, Table 4 indicates that the presence of a buried layer somewhat affects the DIBL value, which is approximately 0.3 V.

FOM in Table 5 depicts the optimum case among four different positions of a 10 nm SiO_2 buried layer in MOSFET, from 30 nm depth to direct contact with the channel. Employing the main parameters in the FOM equation, the parameters that need to be raised are placed in the numerator, and the parameters that need to be down are placed in the denominator. FOM values of each position are increased with the buried layer shifted up. As 30 nm, FOM is 249.9 $\times 10^8$, considered a smaller value compared with the FOM of the buried layer in direct contact with the channel, which has a 3011.1×10^8 value, which is investigated as an optimum value among the three positions.

Table 5: FOM of parameters at (30 nm, 20 nm, 10 nm, and direct contact) depths.

	30 nm Depth	20 nm Depth	10 nm Depth	Direct Contact
FOM	249.9×10^8	456.6×10^8	1059.2×10^8	3011.1×10^8

Figure 6 depicts the electric field distribution within the bulk of a 20nm MOSFET, as simulated by Silvaco ATLAS.

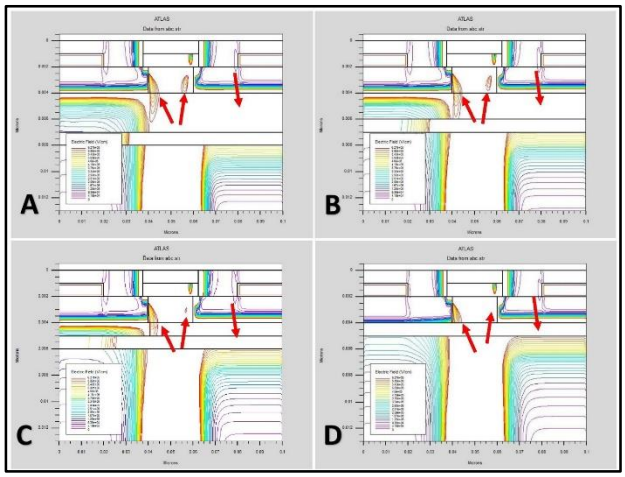

Figure 6. Electric field distribution in the bulk of 20 nm MOSFET with 10 nm SiO_2 buried layer at depth (30 nm, 20 nm, 10 nm, and direct contact with the channel).

The electric field diagrams are presented in Figures 6(A-D), depicting a device with a 10 nm thickness SiO_2 buried layer at 30 nm depth beneath the channel, and shifted up to become in direct contact with the channel. The shift up 10 nm SiO_2 buried layer resulted in a considerable alteration of the electric field distribution. At 30 nm depth, as shown in Figure 6(A), the electric field distribution increases due to the fringing fields that are concentrated at the drain and source region, and the electric field is suppressed above the SiO_2 buried layer at the drain side (right side). Compared with Figure 6(A), Figures 6(B) and 6(C) depict the shift up the buried layer to 20 nm depth and 10 nm depth respectively, fringing fields are decreased within each step, and the electric field is confined at source side above SiO_2 buried layer, and suppressed above SiO_2 buried layer at the drain side. Finally, when the buried layer is in direct contact with the channel, fringing fields are diminished at the drain side, and the electric field distribution is decreased significantly at the source region, which could increase the electric field at the source-channel junction. The decay of fringing fields decreases the electric field intensity at the drain side, which protects the device from failure by raising the breakdown voltage and decreasing the leakage current.

Figure 7 illustrates the electric field distribution along the channel of a 20nm MOSFET under different situations, shifted up the 10 nm thickness buried layer from 30 nm depth to direct contact with the channel position. The electric field behaviour when a buried layer at 30 nm depth to 10 nm depth, displays a significant peak at the source end of the channel, due to carrier injection from the source to the drain.

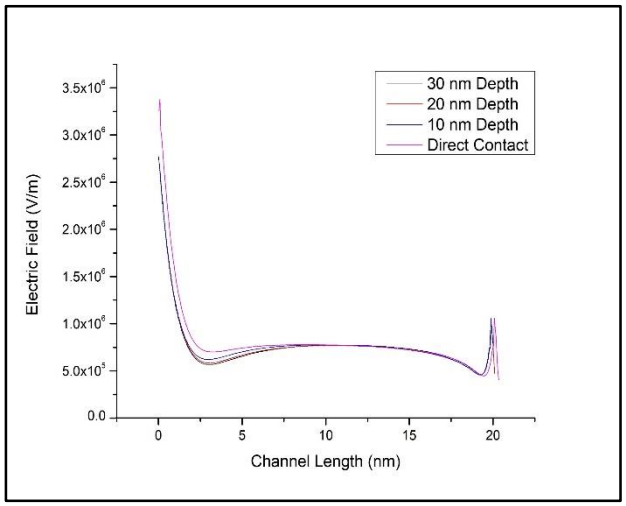

Figure 7. Electric field distribution along the channel of 20 nm MOSFET with 10 nm SiO_2 buried layer at depth (30 nm, 20 nm, 10 nm, and direct contact with the channel).

The electric field decreases throughout the channel but remains extremely high in the central area. A secondary small peak is found at the drain end, due to high-field regions near the drain. The buried layer is in direct contact with the channel, it is noticed that the peak of the electric field is higher than the three previous positions due to the position of the buried layer which redirects the electric field from the source region to the source end with the channel, the electric field is decreased between source and region and it is almost equal for the four case. Another peak in the drain region indicates that the electric field is less than three previous case positions. Shifting up the positions of the 10 nm thickness buried layer reduced the electric field intensity in crucial areas (source and drain), enhancing reliability by mitigating hot carrier effects and decreasing the possibility of failure of the device.

4. Comparative Study

The performance of this work was compared to the other structure, as summarized in the Table 6, along with citations from previously published studies. The table demonstrates that the proposed structure exhibits commendable performance, taking into account the gate length and supply voltages employed. The references [39-41] utilize identical gate lengths but different MOSFET topologies, and the references [42, 43] depict the SOI-MOSFETs.

The comparative analysis of several MOSFET topologies, utilizing the supplied data, exposes different trade-offs among critical device characteristics, including V_{th}, I_{on}, I_{off}, I_{on}/I_{off} ratio, breakdown voltage, and DIBL. All devices possess a uniform channel length of 20 nm to facilitate equal comparison. The MOSFET design, including a 10 nm buried SiO_2 layer, demonstrates a modestly decreased V_{th} to 0.454 V and enhanced I_{on} to 2.09×10^{-3} A/m compared to the conventional design without a buried layer. This is accompanied by a little escalation in I_{off} to 1.01×10^{-10} A/m. The incorporation of the buried layer markedly increases the breakdown voltage from 85.09 V to 167.4 V, indicating enhanced vertical electric field isolation. The direct contact position of buried layer structure exhibits an optimal balance, characterized by a marginally elevated V_{th} to 0.464 V, minimal I_{off} of 5.15×10^{-11} A/m, a substantial I_{on}/I_{off} ratio of 3.62×10^{7}, and the highest breakdown voltage of 1186.7 V, rendering it exceptionally robust and appropriate for high-voltage, low-power applications. Nonetheless, its DIBL of 0.307 V/V remains modest, comparable to previous buried layer configurations, suggesting that although vertical field suppression has improved, horizontal electrostatic control is not markedly better. Conversely, conventional gate topologies exhibit remarkably low V_{th} of 0.043 V, yielding the highest I_{on} of 2.36×10^{-3} A/m; nevertheless, this is accompanied by substantially elevated I_{off} to 1.3×10^{-10} A/m and a suboptimal I_{on}/I_{off} ratio of 1780, which constrains energy efficiency. The unconventional gate engineering structure enhances the I_{on} to 2.66×10^{-3} A/m and marginally decreases I_{off} to 0.11×10^{-9}A/m, resulting in a little improvement in the switching ratio to 2285; nonetheless, it continues to exhibit a very low V_{th} of 0.037 V, which raises issues for low-power design.

Gate engineering substantially diminishes DIBL to 0.154 V/V, demonstrating its efficacy in enhancing short-channel electrostatics. The DG-MOSFET, although theoretically advantageous due to its dual-gate control,

functions at a significantly reduced drain voltage of 0.1 V and exhibits a notable decline in performance metrics, characterized by a low I_{on} to 0.27×10^{-3} A/m, a relatively high I_{off} of 1.9×10^{-10} A/m, and a suboptimal I_{on}/I_{off} ratio of 136.4, suggesting restricted applicability in high-performance contexts. The GAA-junctionless device exhibits superior electrostatic control, characterized by the lowest DIBL of 0.112 V/V and the greatest V_{th} of 0.72 V, indicating exceptional suppression of SCEs. Nonetheless, it exhibits suboptimal performance for I_{on} with 1.3×10^{-6} A/m and I_{off} with 6.33×10^{-8} A/m, resulting in diminished applicability for rapid-switching logic circuits, despite a satisfactory I_{on}/I_{off} ratio of 2.07×10^{6}.

The high-low resistance BOX (HLRB) SOI-MESFET has a V_{th} of 0.4 V, facilitating an I_{on} of 6.1×10^{-3} A/m, so rendering it appropriate for high-speed applications. Nonetheless, this benefit is surpassed by a significantly elevated I_{off} of 4×10^{-5} A/m, yielding a small I_{on}/I_{off} ratio of 152.5. Furthermore, the breakdown voltage is constrained to 27 V, signifying diminished robustness for high-voltage operation. In contrast, the high voltage trench (HVT) MOSFET exhibits a markedly elevated V_{th} of 1.7 V, which effectively mitigates leakage, resulting in an exceptionally low I_{off} of 1×10^{-9} A/m. Despite its I_{on} being significantly lower at 0.16×10^{-3} A/m in comparison to the HLRB SOI-MESFET, the resultant I_{on}/I_{off} ratio of 1.6×10^{5} is markedly superior, showing its energy efficiency and suitability for low-power, standby-sensitive applications. Additionally, the HVT MOSFET demonstrates a markedly elevated breakdown voltage of 78 V, suggesting more resilience to high electrical fields, and a low DIBL value of 0.126 V/V, signifying greater electrostatic control and improved resistance to SCEs.

Table 6: Comparative study of our works with other MOSFET topologies.

Structures	L_g (nm)	V_D (V)	V_{th} (V)	I_{on} (A/m)	I_{off} (A/m)	I_{on}/I_{off}	Breakdown Voltage (V)	DIBL (V/V)
Without a buried layer [22]	20	0.8	0.462	2×10^{-3}	8.51×10^{-11}	2.37×10^{7}	85.09	0.3089
10nm thickness SiO_2 buried layer (this work)	20	0.8	0.454	2.09×10^{-3}	1.01×10^{-10}	2.0×10^{7}	167.4	0.307
Direct contact position (this work)	20	0.8	0.464	1.86×10^{-3}	5.15×10^{-11}	3.62×10^{7}	1186.7	0.307
Conventional gate arch. [39]	20	0.8	0.043	2.36×10^{-3}	0.13×10^{-9}	1780	-	0.227
Non-conventional gate arch. (Gate Engineering) [40]	20	0.8	0.037	2.66×10^{-3}	0.11×10^{-9}	2285	-	0.154
DG-MOSFET [40]	20	0.1	0.289	0.27×10^{-3}	0.19×10^{-9}	136.4	-	-
GAA-Junctionless [41]	20	-	0.72	1.3×10^{-6}	6.33×10^{-8}	2.07×10^{6}	-	0.112
HLRB-SOI-MESFET [42]	50	-	0.4	6.1×10^{-3}	4×10^{-5}	152.5	27	-
HVT SOI-MOSFET [43]	50	-	1.7	0.16×10^{-3}	1×10^{-9}	1.6×10^{5}	78	0.126

In summary, although gate-engineered and conventional architectures seek superior performance, they compromise I_{off} and V_{th}. The GAA-junctionless and DG-MOSFETs highlight control and simplicity, although they exhibit limitations in I_{on} and I_{off}. The HLRB-SOI-MESFET provides enhanced Ion and is ideal for high-speed applications; nevertheless, it suffers by significant leakage and restricted breakdown tolerance. Conversely, the HVT SOI-MOSFET

emphasises energy efficiency and strong reliability, demonstrating superior leakage reduction, Ion/Ioff ratio, and breakdown voltage, but this comes at the cost of diminished driving capability.

The MOSFET with a buried layer at direct contact position with the channel stands out as the most balanced solution, providing robust drive performance, superior leakage suppression, high breakdown voltage, and excellent electrostatic characteristics, establishing it as a competitive candidate for future scaled and power-efficient technologies.

5. Conclusions

This study models a nano-scale MOSFET using Silvaco ATLAS, with a 20 nm channel length, an HfO_2 gate dielectric, and a 10 nm thick SiO_2 buried layer implanted 30 nm below the channel. In the first scenario, the buried layer thickness is increased from 10 nm to 50 nm. Compared to a standard MOSFET without a buried layer, this increase in thickness leads to higher leakage current due to enhanced fringing fields at the drain side, negatively impacting the I_{on}/I_{off} ratio. Additionally, the breakdown voltage is highest when the buried layer is 10 nm thick. In the second scenario, the MOSFET's performance is improved by optimizing the buried layer thickness. Specifically, the 10 nm buried layer is adjusted to directly contact the channel, significantly reducing leakage current by minimizing fringing fields. This adjustment enhances the I_{on}/I_{off} ratio and substantially boosts the breakdown voltage. The study concludes that a thicker SiO_2 buried layer, located farther from the channel, delivers poorer performance compared to a thinner buried layer positioned closer. The optimal configuration is achieved with a 10 nm SiO_2 buried layer directly in contact with the channel, providing superior results for the 20 nm MOSFET.

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