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NEW SYMMETRICAL MULTILEVEL INVERTER WITH REDUCTION OF SWITCHES

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ABSTRACT: - New symmetrical multilevel inverter topology with reduced number of power electronic switches is introduced in this paper, which results in reduction of installation area, converter cost, losses, and have simplicity of control system. The proposed topology consists of series connected sub multilevel inverter blocks. Principles of operation and switching functions are well analyzed. Simulation results are provided for seven levels inverter to validate the proposed theory.

Keyword: Cascade Multilevel Inverter (CMLI), Symmetrical Multilevel Inverter, Total Harmonic Distortion (THD).

1. INTRODUCTION

Multilevel inverters generate output voltage from several levels of dc voltages with negligible distortion comparing with conventional inverters [1, 2]. The term multilevel began with the three-level inverter [3, 4]. Multilevel inverters were introduced in 1975 [5, 2]. Power electronic multilevel inverters are becoming more popular for various industrial applications. Medium to high-voltage applications are receiving great attention that is seen in static reactive power compensation and adjustable-speed drives [6, 7].

The most common multilevel inverters are diode clamped MLI (DC-MLI), flying capacitor MLI (FC-MLI) and the cascaded multilevel inverter (CMLI), H bridge inverters with separate DC sources. Among these three configurations cascaded H bridge inverters uses less components for a given number of levels [8].

The three aforementioned structures have been used in various hybrid applications [8,9]. Another slightly different multilevel design came up; whereby parallel connection of inverters [10]. All these topologies have different mechanism to provide voltage levels.

Soft-switching methods have been used for efficiency enhancement and switching loss reduction. Subsequently, several multilevel inverter topologies have been introduced [11, 3]. The better power quality, low switching losses, reduced dv/dt stress, less common mode voltage and the compatibility for electro-magnetic and high-voltage are some advantages of multilevel inverters over the traditional two-level voltage converter [3, 7].

It is noteworthy that multilevel inverters have some disadvantages over the two-level inverter. Multilevel inverters require more power semiconductor switches. Even though low-voltage-rated switches can be utilized, each and every switch has to be provided with gate driver and protection circuit. Such requirements lead to more complexity in power circuits and control schemes. Beside that the overall system becomes more expensive. Therefore, number of switches and gate driver circuits are very prominent in inverters design [7].

To produce more steps with reduced number of switches, new symmetrical multilevel inverter topology is presented in this paper. Working principles and switching functions are analyzed Finally, Simulation results are provided for validity verification

1- THE PROPOSED MULTILEVEL INVERTER

Number of switches is the most important criterion in multilevel inverters technology. It defines the reliability, cost, circuit size, installation area and control complexity. The number of required power switches against required output voltage levels is the very important element in the design. To generate more output levels with fewer switches, the topology in Fig. 1 is presented. As depicted is Fig. 1, power switches are connected in series, such connection makes the switches less stressed and over voltage condition is overcome.

In Table 1 switching states are listed with their respective output voltages. For more output voltage levels one DC power supply is used.

The number of output phase voltage levels in proposed topology is defined by:

$$N_{Step} = 2N + 1 \quad (1)$$

Where N is the number of separate dc sources (photovoltaic modules or fuel cells) and the maximum output voltage (V_{omax}) of this proposed multilevel inverter is:

$$V_{omax} = (\frac{N_{Step}-1}{2})Vdc \quad (2)$$

Also, the number of power switches required in the proposed symmetric multilevel inverter is given by:

$$N_{Switches} = N_{\text{step}} + 1 \quad (3)$$

2- SIMULATION RESULTS

It is well know that multilevel inverters are assessed based on the load current harmonics distortion. To achieve an inverter with better performance harmonics distortion need be diminished.

For analysis purpose harmonic performance in the proposed topology was compared with it's in other topologies. Several techniques have been introduced for harmonics measurement. The total harmonic distortion (THD) is considered one of widely used techniques in power inverters design. It calculates the quantity of harmonic components in the output waveform.

As mentioned earlier, the configuration in Fig. 1 is made for up to N voltage level inverter. To reach any desired number of output levels, power circuit can be extracted from Fig. 1. The working principles never change with number of voltage levels.

To ensure its feasibility, symmetrical seven levels inverter shown in Fig. 2 was simulated in Matlab Simulink power blockset software. The parameters selected for testing are: (a) An LC filter with C=10μf and L =0.5mH and (b) A resistive load of 100Ω. Table 2 shows the ON switches lookup table.

Specific control strategy is applied to make load voltage waveform close to the reference signal. Phase Dissipation (PD) has taken place as modulation technique.

The output waveforms and their corresponding Fourier Spectrums are shown in Fig. 3, 4 and 5 are the filter input voltage, load voltage and load current, respectively.

3- CONCLUSIONS

A new configuration of symmetrical multilevel inverter has been proposed in this paper. Flexibility in the selection of the inverter output voltage levels with minimized number of switches makes the topology more advantageous. Feasibility of the presented technique is noticed also in the measured THD. The way is paved for designers to not miss any generated voltage level. The output voltage was achieved with fewer switches and less voltage drop. Based on the provided simulations results, the proposed inverter topology generates high-quality output voltage waveform. In addition the harmonic components of output voltage and current are low

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Table.1. N Switches Look-Up Table

Switches states	V_{out}						
	$-NV_{dc}$	…….	$-V_{dc}$	0	$+V_{dc}$	…….	$+NV_{dc}$
S_1	0ff	off	off	off	on	on	on
S_2	0ff	0ff	off	on	on	on	on
S_3	on	on	on	off	0ff	off	off
S_4	on	on	on	on	0ff	off	off
S_5	off	off	on	off	on	off	off
S_6	on	…….	off	off	off	…….	on
…….	….	…….	….	……	….	…….	….
S_{2N+1}	off	…….	off	off	off	…….	off
S_{2N+2}	on	…….	off	off	off	…….	on

Table.2. Values of V_O for State of Switches

Switches states	Vout						
	-150	-100	-50	0	50	100	150
S_1	off	off	off	off	on	on	on
S_2	off	off	off	on	on	on	on
S_3	on	on	on	off	off	off	off
S_4	on	on	on	on	off	off	off
S_5	off	off	on	off	on	off	off
S_6	on	on	off	off	off	on	on
S_7	off	on	off	off	off	on	off
S_8	on	off	off	off	off	off	on

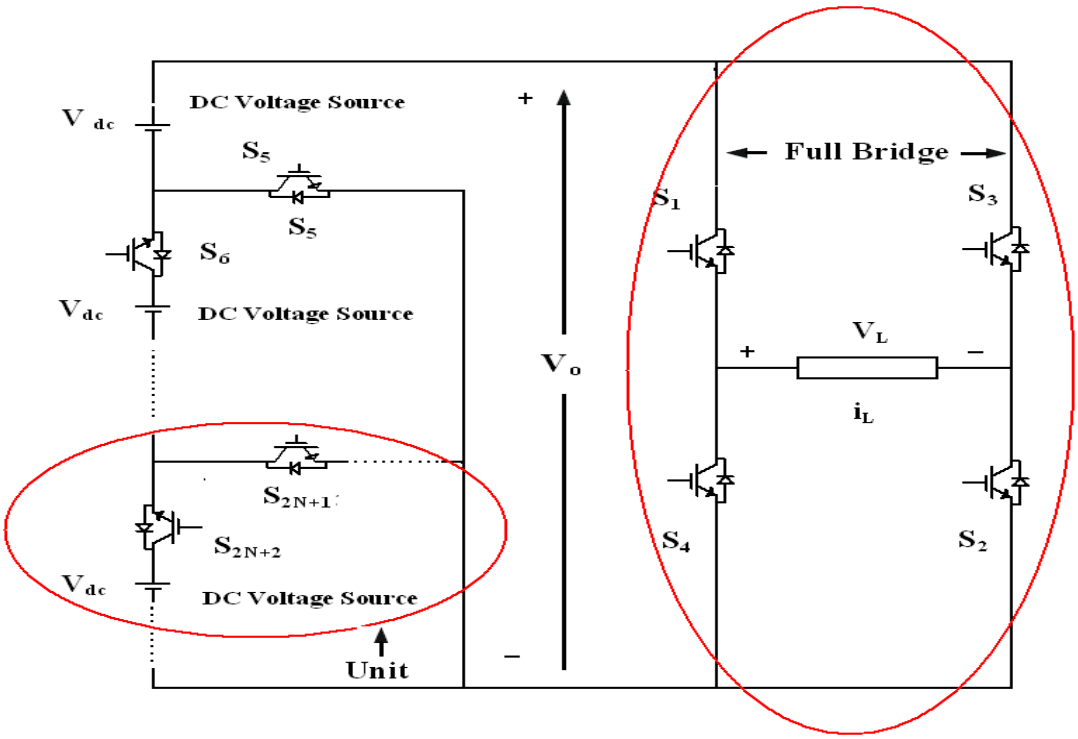

Fig.1. Suggested basic topology for a symmetrical inverter.

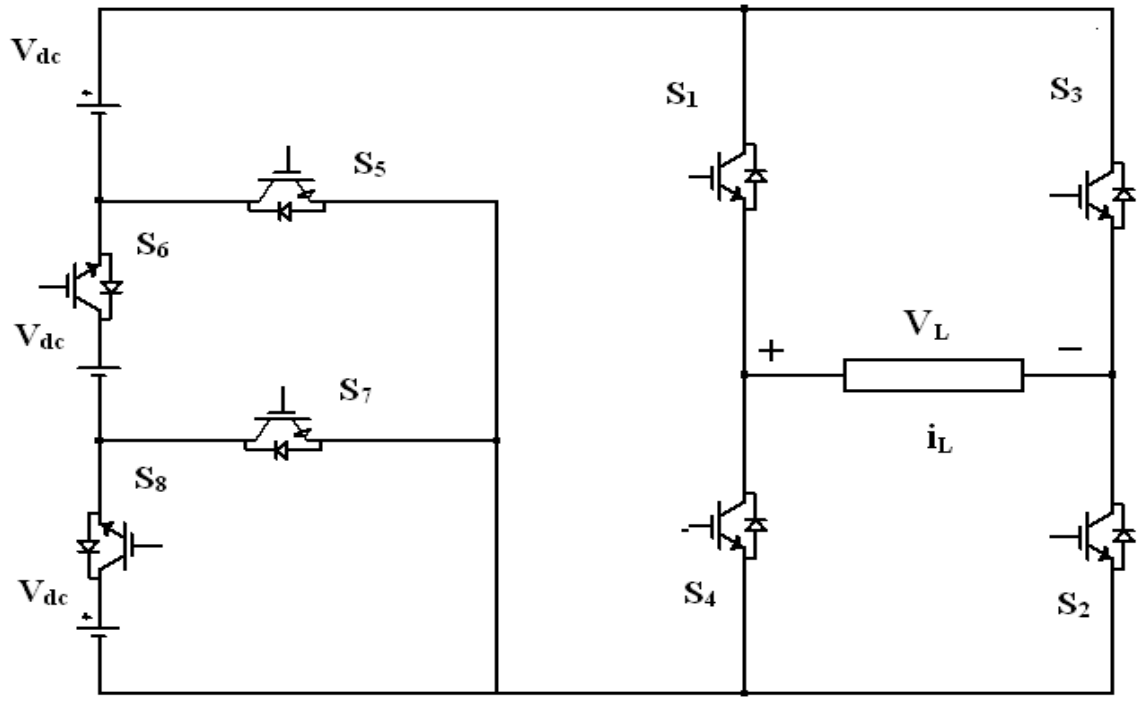

Fig. 2. 7-Level symmetrical MLI

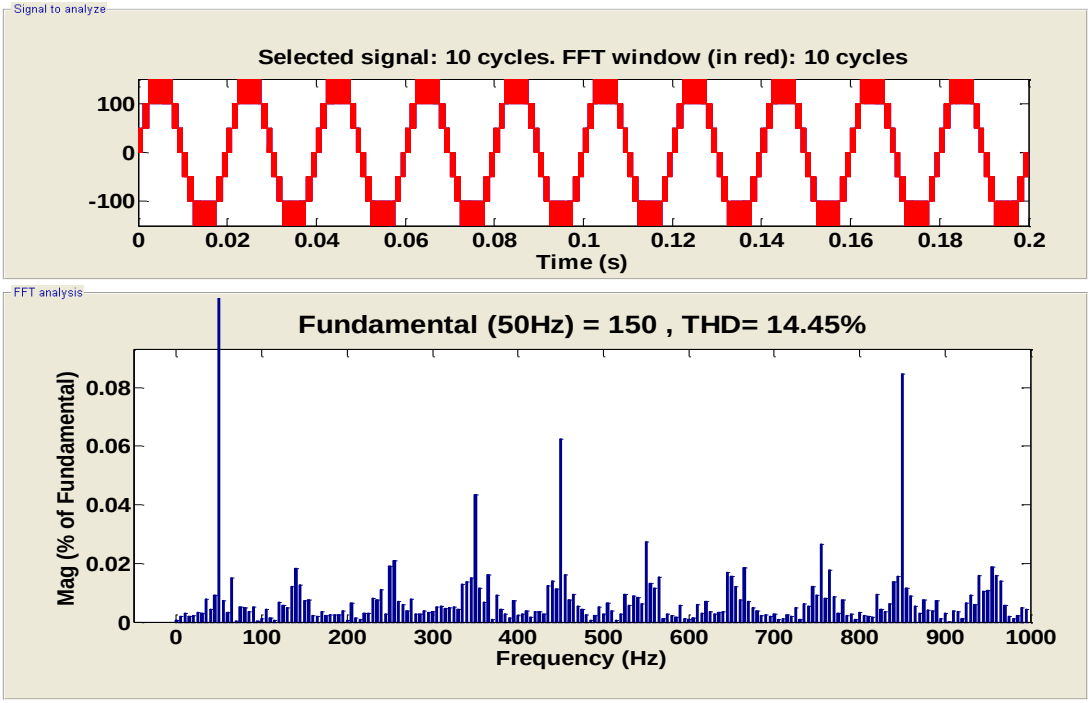

Fig. 3. Simulated input voltage to filter V_{in} and corresponding Fourier spectrum

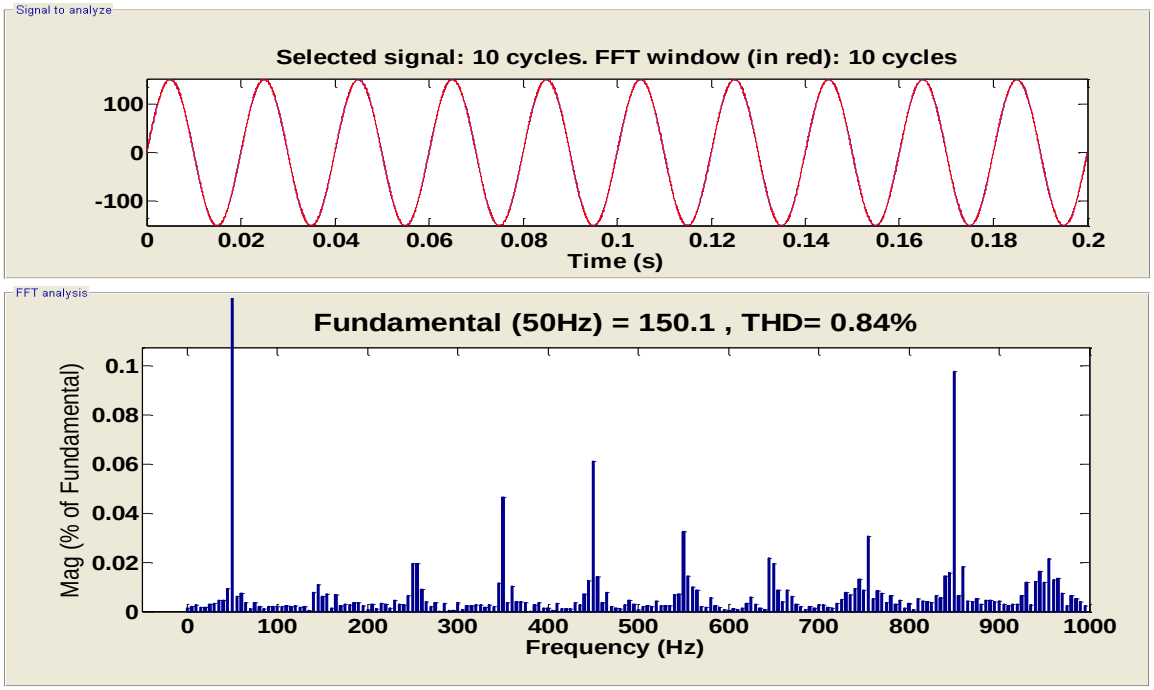

Fig. 4. Simulated output voltage (V_L) and corresponding Fourier spectrum

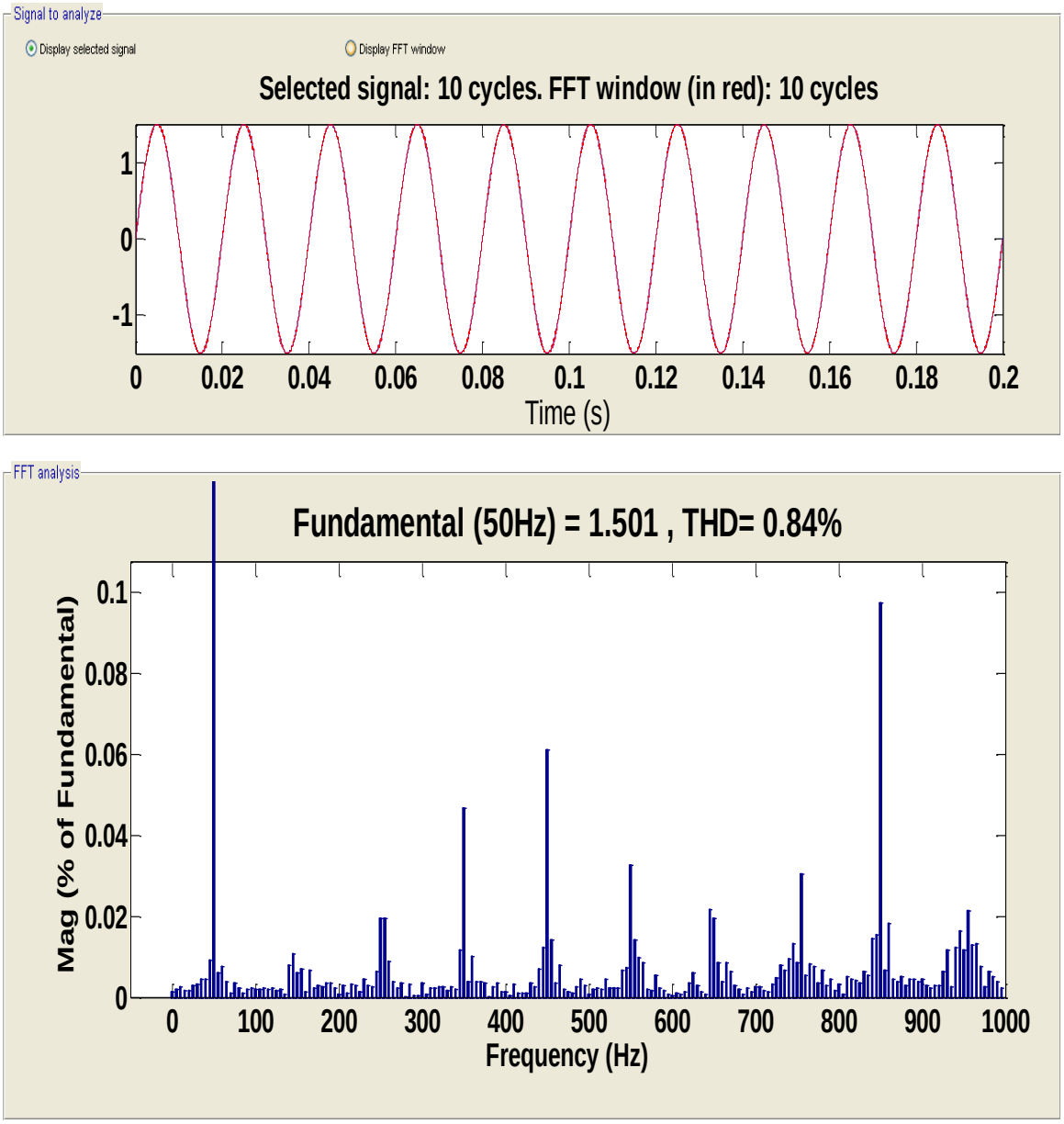

Fig. 5. Output current (I_L) and corresponding Fourier spectrum

عاكس جديد متعدد المستويات متماثل المصدر مع تقليل المفاتيح

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الخلاصة

نوع جديد من عاكس متعدد المستويات متماثل المصدر مع تقليل عدد من المفاتيح الالكترونية المتعرف عليه في هذا البحث, حيث النتائج عن هذا البحث تقليل في المساحة المستخدمة , تقليل في الكلفة , تقليل في الخسائر,وبساطة التصميم في السيطرة عليه.هذا النوع الجديد يتكون من قطع من عاكسات متعدة المستويات مربوطة على التوالي .
مبادى العمل وظائف المفاتيح تم تحليلها. نتائج المحاكاة لنموذج سبع مستويات تم تحقيها للتاكد من صحة البحث الموسوم