IMPLEMENTATION OF STORAGE DEVICE (RAM) USING MULTISIM

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ABSTRACT:- Read access memory (RAM) considers an important part in several systems such as computer and communication systems; and there is several applications software that used for implements the digital circuits of RAM. In this project, multisim 9 application software was used to implement and simulate several logic circuits of RAM with many sizes at which implement RAM circuit from sub RAM. Also, it may be prepared as apart of equipments for the airborne computer system.

INTRODUCTION

(Random access memory) or read/write memory is a type of memory that provides direct access to any byte on the chip. This "byte addressing" means that the contents of any byte can be read or written without regard to the bytes before or after it. In addition, read and write speeds are symmetrical. It takes no longer to write a byte than it does to read one. [1][2] RAM (also referred to as read-write memory, RWM) is considered volatile storage because its contents are lost when the power is removed.[3] Computer and other types of system require the permanent or semi permanent storage of large amounts of binary data. Memory is the portion of a system which used for storing binary data in large quantities. Memory unit is a device to which binary information is transferred for storage and from which information is available when needed for processing .Binary information received from input device is stored in memory and information transferred to an output device is taken from memory.

There are two categories of memories in current use semiconductor and magnetic, within each category are a variety of memory types, generally the semiconductor memories are used for smaller capacity and faster access applications. The various types of magnetic

memories are used for larger capacity bulk storage but it generally takes much longer to access information.[4]

In fact, RAM consists of the following connections: [3][5]

❖ Address lines define the memory location to be selected for reading or writing.

❖ Input/output data lines define the data to write to or read from memory.

❖ Write enable (WE) is a control input that selects between the memory read and write operations (usually active low).

❖ Output enable (OE) is a control input that enables the output buffer for reading data from the memory (usually active low).

❖ Chip select (CS) selects the memory (usually active low).

❖ Power supply provides the necessary power to operate the circuit.

MULTISIM 9

Multisim 9 provides schematic capture and simulation, including optional patented co-simulation of SPICE and VHDL, for the professional designer. Also, included in the Electronics Workbench suite are Ultiboard for advanced PCB Layout and Ultiroute for grid-based or gridless auto routing. Multisim as a part of the Circuit Design Suite combines the intuitive environment with NI Ultiboard layout. This integrated tool chain for circuit capture, simulation, and layout allows you to use this product in a wide range of classes to: [6]

- Simulate and analyze circuits for homework and pre-lab assignments
- Explore breadboard in 3D before lab sessions.
- Create printed circuit boards (PCBs) for design projects.

THE DECODER

A binary code of n bit is capable of representing up to 2^n distinct elements of the coded information. A decoder is a combinational circuit that converts binary information from the n coded inputs to a maximum of 2^n unique output. The decoders in this case are called n-to-m line decoders, where m $<=$ 2^n. their purpose is to generate the 2^n binary combination of the n input variables. A decoder has n inputs and m outputs and also is

referred to as an n*m decoder. The logic diagram of a 3-to-8 decoder is shown in figure (1) the three data inputs, A0,A1,A2,are decoded into eight outputs, each output represent one of the combinations of the three binary input variables. The three inverters provide the complement of the inputs and each of the eight AND gates generate one of the binary combination. A particular application of this decoder is a binary-to- octal conversion. The input variables represent the eight digit of the octal number system. However, a 3-to-8 line decoder can be used for decoding any 3-bit code to provide eight outputs, one for each combination of the binary code.[7] When the enable input E is equal to 0, all the outputs re equal to 0 regardless of the values of the other three data inputs. The three x's in the table designate don't-care conditions. When the enable input is equal to 1, the decoder operates in normal fashion. For each possible input combination there are seven outputs that are equal to 0 and only one that is equal to 1 the output variable whose value is equal to 1 represents the octal number equivalent of the binary number that is available in the input data line*s*. [2].

INTERNAL CONSTRUCTION OF RAM

RAM has three basic building blocks, namely an array of memory cells arranged in rows and columns with each memory cell capable of storing either a '0' or a '1', an address decoder and a read/write control logic.[8] The internal construction of a random-access memory of m words and n bits per word consists of m*n binary storage cells and associated decoding circuits for selecting individual words. The binary storage cell is basic building block of memory unit. The equivalent logic of a binary cell that stores one bit of information .the storage part of the cell is modeled by an S-R latch with associated gate. Actually, the cell is an electronic circuit with four to six transistors. never the less ,it is possible and convenient to model it is using logic symbol .A binary storage cell must be very small in order to be able to pack as many cell as possible in small area available in the integrated circuit chip. The binary cell stores one bit in its internal latch. The select input enables the cell for reading or writing and read/write input determines the cell operation when it is selected. A (1) in the read/write input provides the read operation by forming a path from the latch to the output terminal. When memory enable is 0 all output of the decoder are (0) none of the memory words are selected. With the memory select at (1) one of four words is selected, dictated by value by the value in the two address lines. Once a word has been selected, the read/write input determine the operation during the read operation, the four bits of the selected word go through OR gates to the output terminals. During the write operation,

the data available in the input lines are transferred into the four binary cells of the selected word. The binary that are not selected are disabled and their previous binary values remain unchanged. When the memory select input that goes into the decoder is equal to (0), none of the words are selected and the contents of all cells remain unchanged regardless of the read /write input. Commercial random access memories may have a capacity of thousands of words and each word may range from 1 to 64 bits .the logical construction of large capacity memory would be a direct extension of the configuration shown here. a memory with 2k words of n bits per word requires k address lines that go into a k*2k decoder .each one of one of the decoder outputs selects one word of n bits for reading or writing.[1] Communication between a memory and its environment is achieved through data input and output lines, address selection lines, and control lines that specify the direction of transfer. A block diagram and internal structure of RAM unit is shown in figures (2) and (3). the n data input lines provides the information to be stored in memory, and the n data output lines supply the information coming out of memory the k address lines provides a binary number of k bits that specify a particular word chosen among the 2^k available inside the memory the two *control* inputs specify the direction of transfer desired. (2).

IMPLEMENTATION OF BINARY CELL

An implementation of binary cell will do at which the R\W select the read from the cell or write to the cell. Each cell store either logic (0) or logic (1). The logic circuit of binary cell is shown in figure (4).

IMPLEMENTATION OF TYPES OF RAMS

a. 4*2bit RAM

In multisim (5) program, we are design RAM 4*2 bit. This RAM contains from 2*4 decode and two addresses input go to this decoder to select one from four words. The decoder is enable with the memory enable input .when the memory enable is equal to logic(0) ,all outputs of the decoder are equal to logic(0) and none of the memory words are selected. when the enable input be logic (1), one of the words is selected, dictated by the value in two address lines and a word has been selected. the read /write input determines the operation. When make read/write equal to logic (1), we will read word from memory and two bits are of selected word go through OR gates to the output terminals. When read/write equal logic (0), write in memory will be done and the data available in the input lines are transferred in to the two

binary cells of the selected word. The binary cells that are not selected are disabled and their previous binary values remain unchanged. When the memory enable input goes into the decoder is equal logic (0), none of the words will select and the contents of all cells remain unchanged regardless, of value of the read/write input. However, 4*2 RAM logic circuit implements by using multisim with two versions: version 5 as shown in figure (5); and version 9 as shown in figure (6).

b. 4*4 bit RAM

Design of 4*4bit Ram consist of (16) binary cells that arranged as an array and 2*4 decoder which give two address lines at its input to select one word from four words. As explained previously, the decoder is enabled by the memory enable input at which when memory enable is logic (0), all output of the decoder are logic (0) and none of the memory words are selected .when memory select at (1), one of from four words is selected, dictated by the value in two address lines, once a word has been selected and the read/write input determine the operation. When read/write equal to one, we will read word from memory and four bits of the selected word go through four OR gates to the output terminal. When read/write equal to zero will write in the memory and the data available in the input lines are transferred into four binary cells of the selected word. The binary cells that are not selected are disabled and their previous binary values remain unchanged. When the memory select input that goes into the decoder is equal to (0), none of the words are selected and the contents of all cells remain unchanged regardless of the read/write input. As a result, figure (7) show this RAM (4*4 bit RAM).

c. 8*2 bit RAM

Design of 8*2 bit Ram required (16) binary cell and 3*8 decoder has three address lines pass to its input to select one from eight words. The decoder, also, is enabled with the memory enable input. However, the figure (8) below show the internal construction of RAM.

d. 8*4 bit RAM

The internal components of this RAM needs (32) binary cells and 3*8 decoder with 3-address lines. One of eight words will select by decoder at which the word width is 4-bit. The important device in this RAM is decoder which use to select chip (activate the chip). The logical circuit of this RAM is shown in the figure (9).

e. 4*8 bit RAM from 4*2 bit RAM

This RAM consists of connection of four 4*2 chips. The (8) inputs and outputs data lines are connect between the four chips; also, each chip have the same 2-bit address; therefore, no decoder use in this RAM. The common CS line and RW control line are use as shown in figure (10) .

f. 4*8 bit RAM from 4*4 bit RAM

By using two chips of 4*4 bit RAM, we can implement a 4*8 bit RAM as shown in figure (11). There is no decoder use in this RAM and the switches (J4-J11) are connects on data lines to give logic 0 or logic 1. J1 and J2 are address lines, J12 is CS line, and J3 is read\write control line. The common CS line and RW control line are connected to the chips and each one has 4 data lines.

g. 8*8 bit RAM from 8*4 bit RAM

By the same way explained above, this RAM consists of two chips of 8*4 bit RAM. Each one connects to 4-bit data lines and two address lines. The logical circuit of this RAM is shown in figure (12) .

h. 4*16 bit RAM from 4*4 bit RAM

This RAM consist from connect of four 4*4 chips, (16) inputs and output data lines are split between the four chips; each chip receive the same 2-bit address and the common CS line and RW control line input. The logical circuit of this RAM is shown in figure (13).

i. 8*4 bit RAM from 4*4 bit RAM

By using two chips of 4*4 bit RAM, we can implement 8*4 bit RAM as shown in figure (14). The 4 input data lines go to all the chips and the outputs must be ORed together to form the common 4 output data lines. The 8 word memory requires a 3-bit address. The 2 bits of the address are applied to the address inputs of all two chips. The other one bit is applied to a 1*2 decoder. The two outputs of the decoder are applied to CS inputs of each chip. The memory is disabled when the memory enable input of the decoder is equal to logic (0), all two outputs of the decoder are equal to logic (0), and none of the chips are selected.

When the decoder is enabled, address bit 3 determine the chip that is selected. If bit 3 is equal to logic (0), the first RAM chip is select. The remaining two address bits select a word within the chip. However, the implementation of several types of RAM are shown in the figures (15),(16)and (17).

CONCLUSIONS

1. For implementing a large circuits (contains large number of components), multisim (version 5 and version 9) unable to run these types of circuits and multisim is limit application program. Also, all logic circuits are added to the library of the program to be standard circuits saved in it.

2. Arising many errors through the run of circuits that built from another circuits and that's because of multisim limitations. Generally, the differences between using multisim and others application programs depends on the number and type of used components (circuit size and technique)

3. It's possible to increase the number of the words in the memory by using two or more RAM chips and it's possible to compute and implements RAMs (practically) under flying conditions as a future works for using in the airborne computer.

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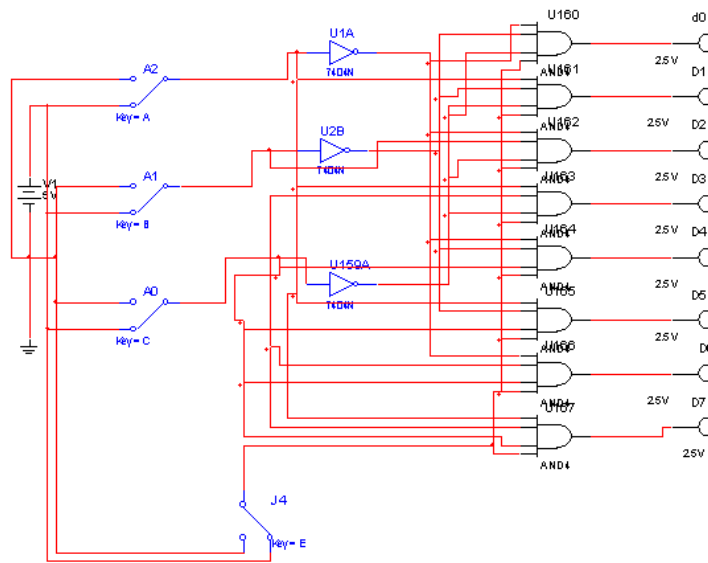
Fig.(1): 3-to-8 decoder logic circuit.
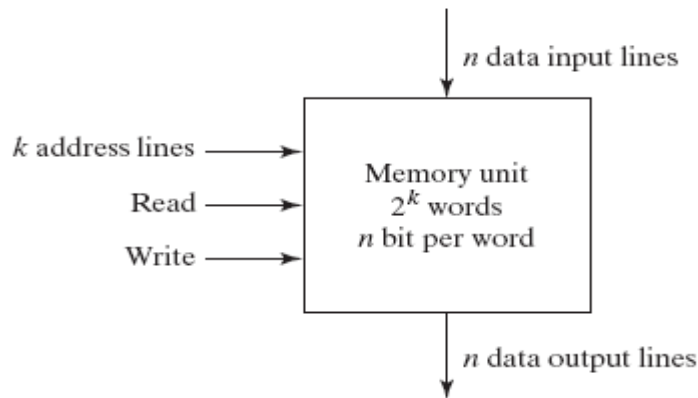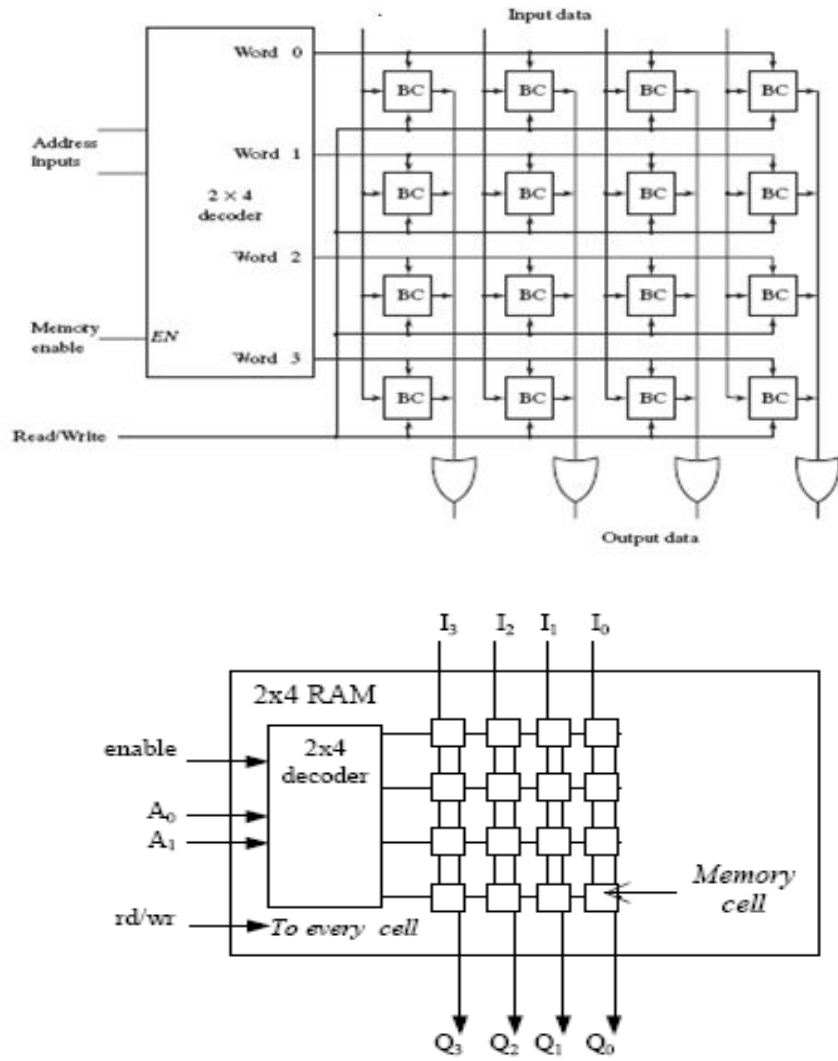

Fig. (2): block diagram of RAM.
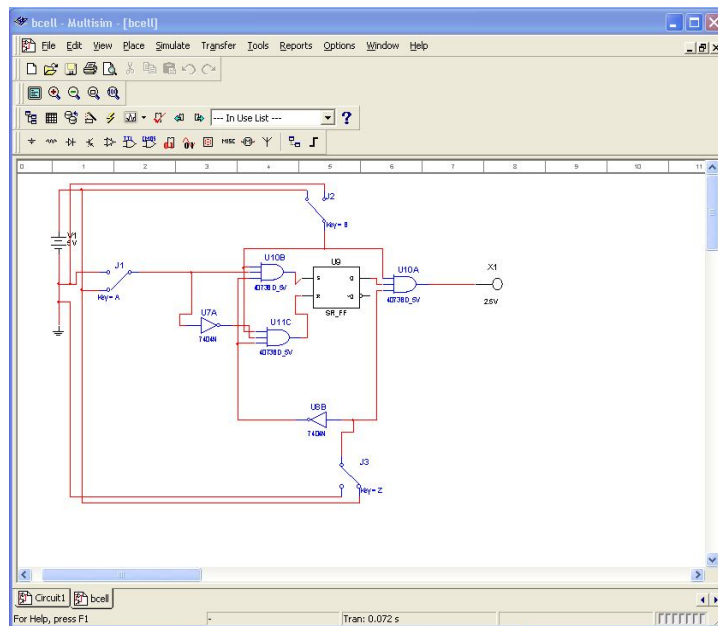
Fig.(3): internal structure of RAM.

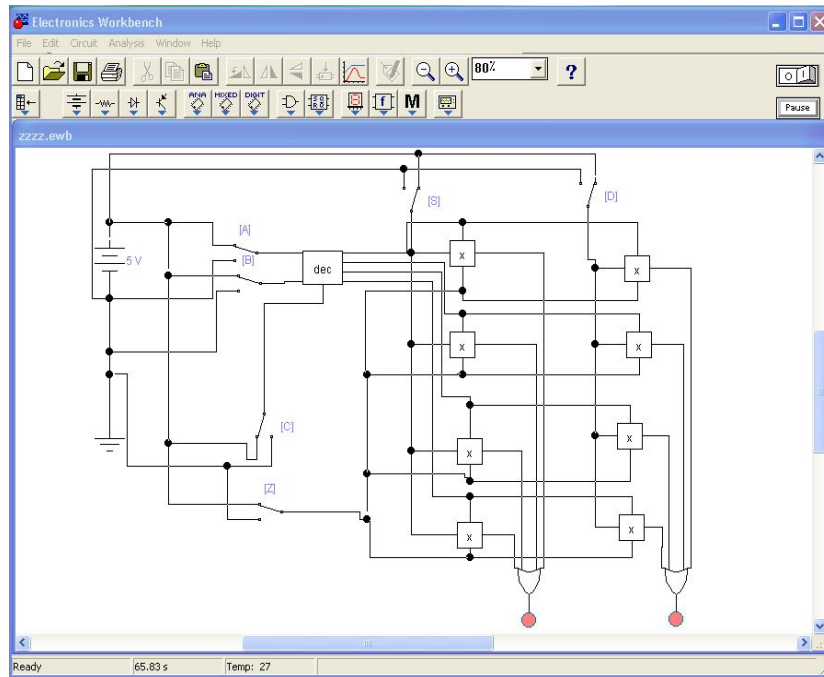**Fig. (4):** logic circuit of binary cell.

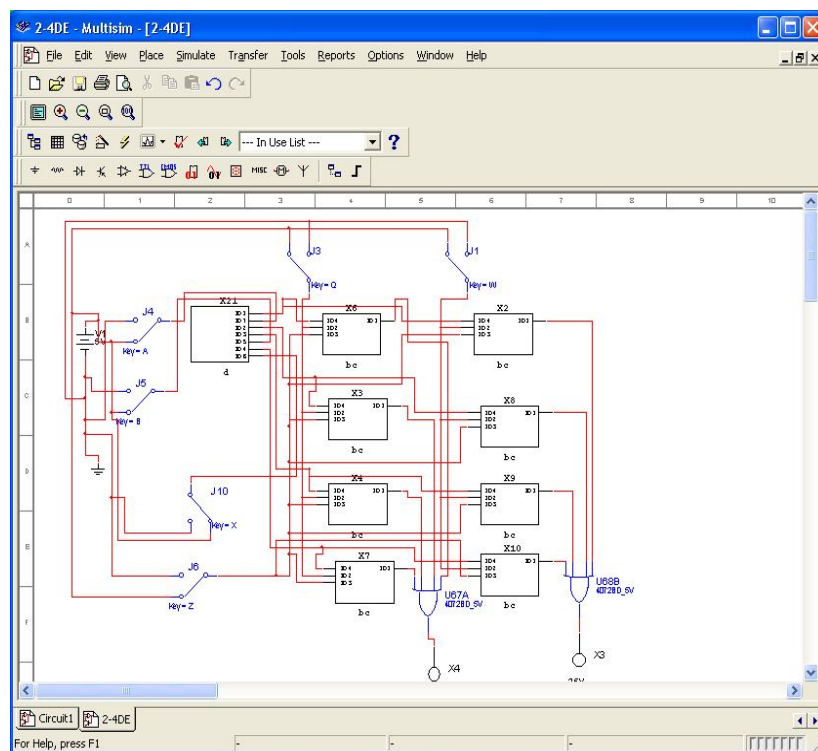**Fig. (5):** 4*2 bit RAM by using EWB version 5.

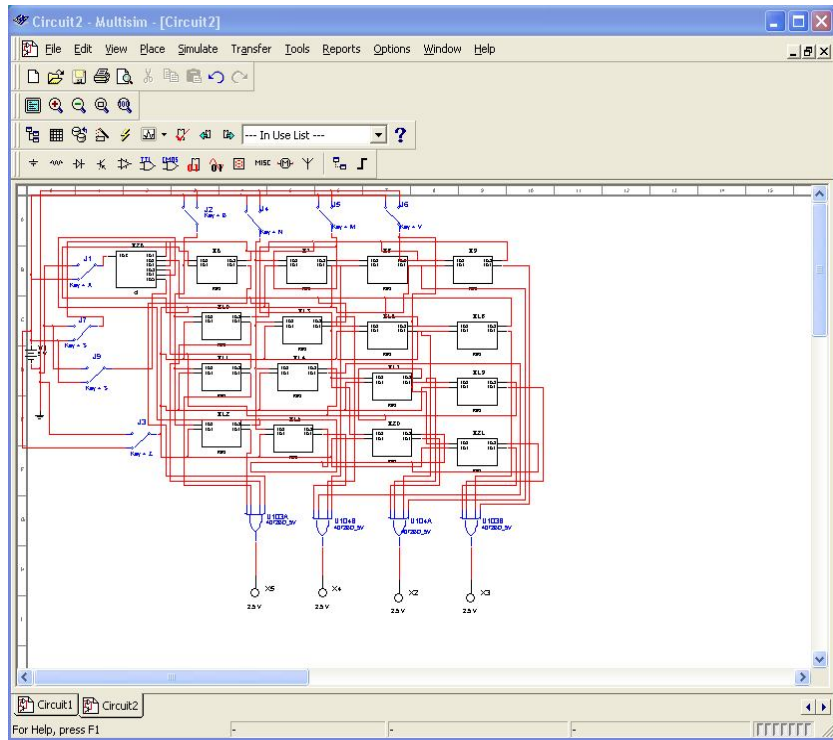**Fig.(6):** 4*2 bit RAM by using multisim version 9.
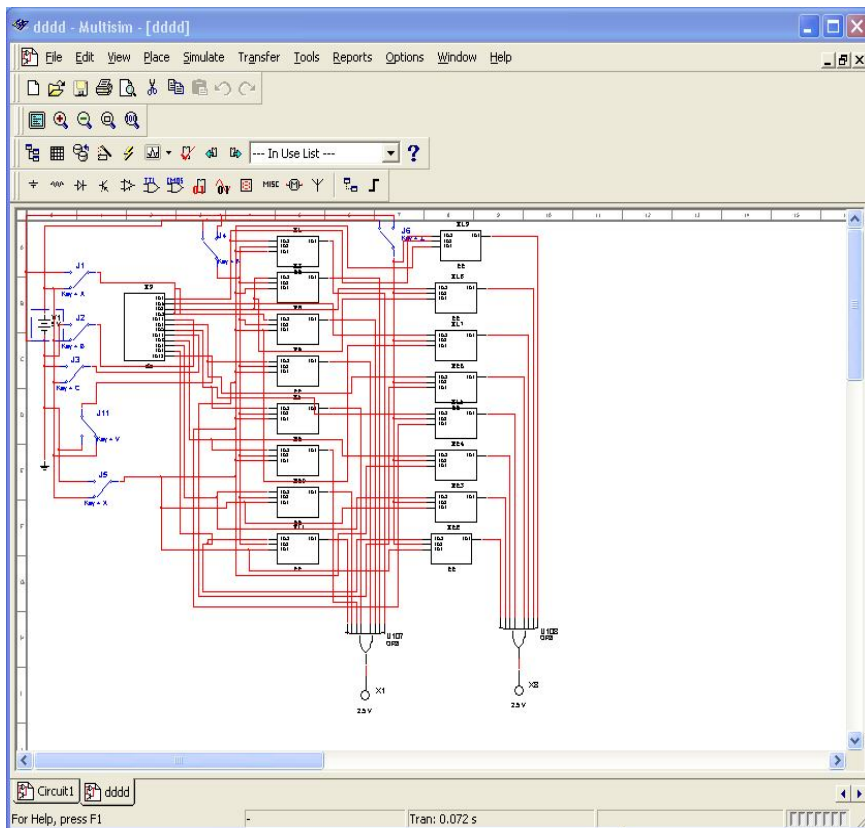
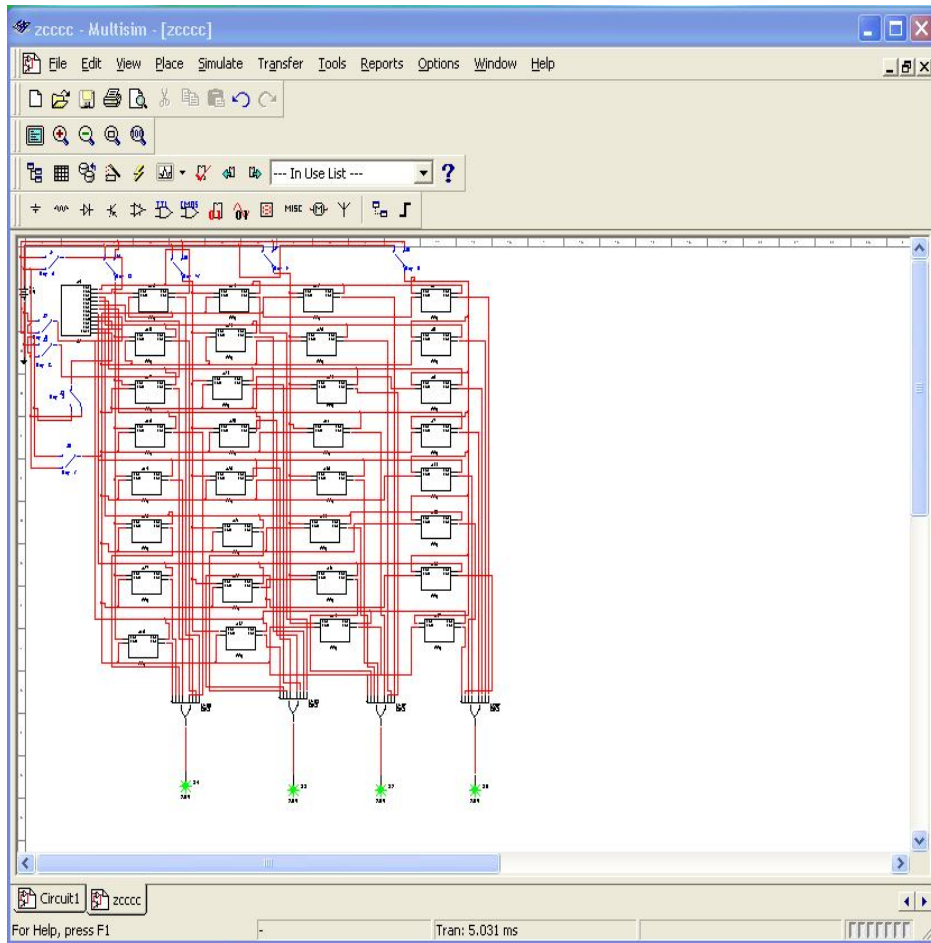**Fig.(7):** 4*4bit RAM logic circuit.

Fig. (8): 8*2bit RAM logic circuit.

Fig. (9): logical circuit of 8*4 bit RAM.
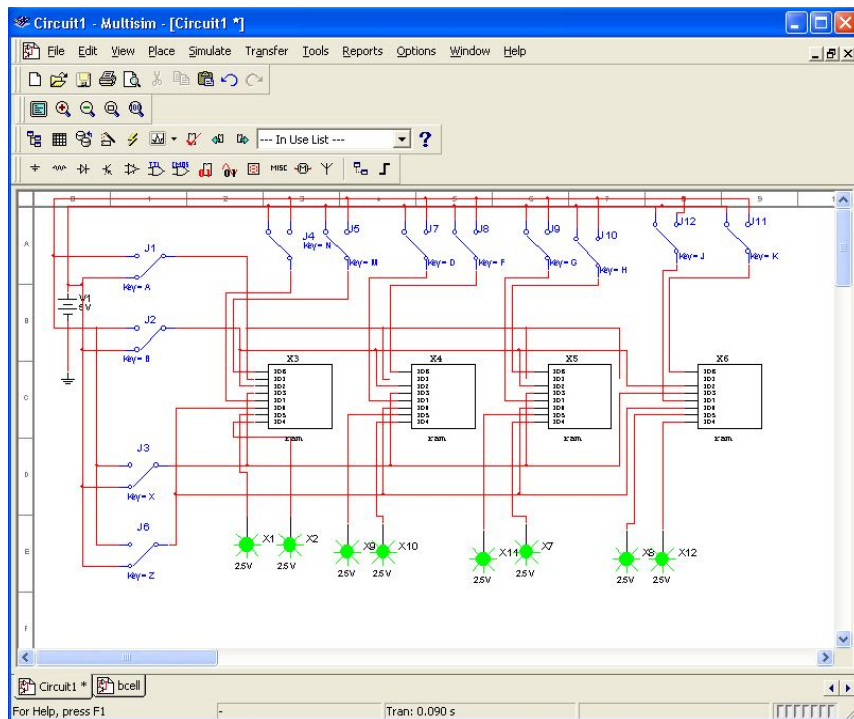
Fig.(10): 4*8bit RAM from 4*2 bit RAM.
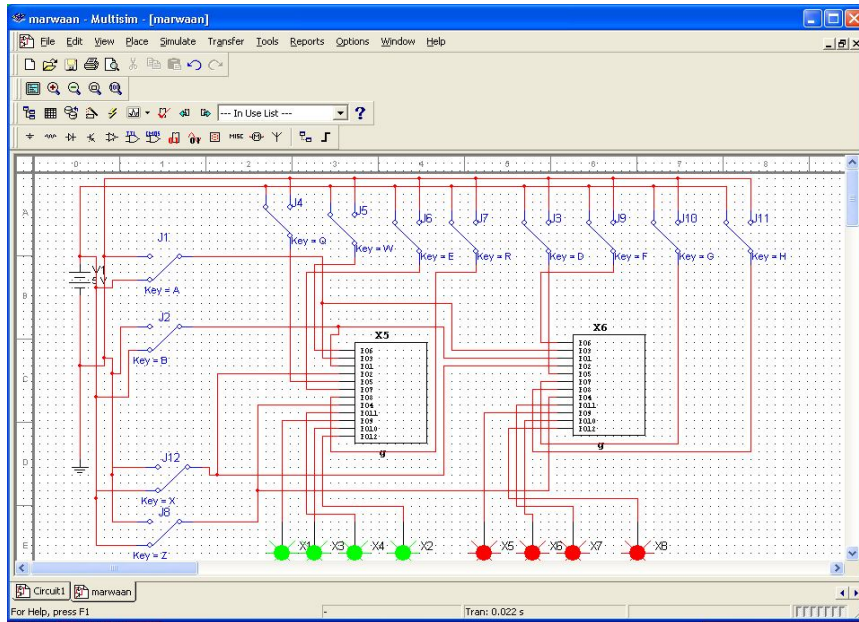
Fig.(11): Design of 4*8 bit RAM from 4*4 bit RAM.
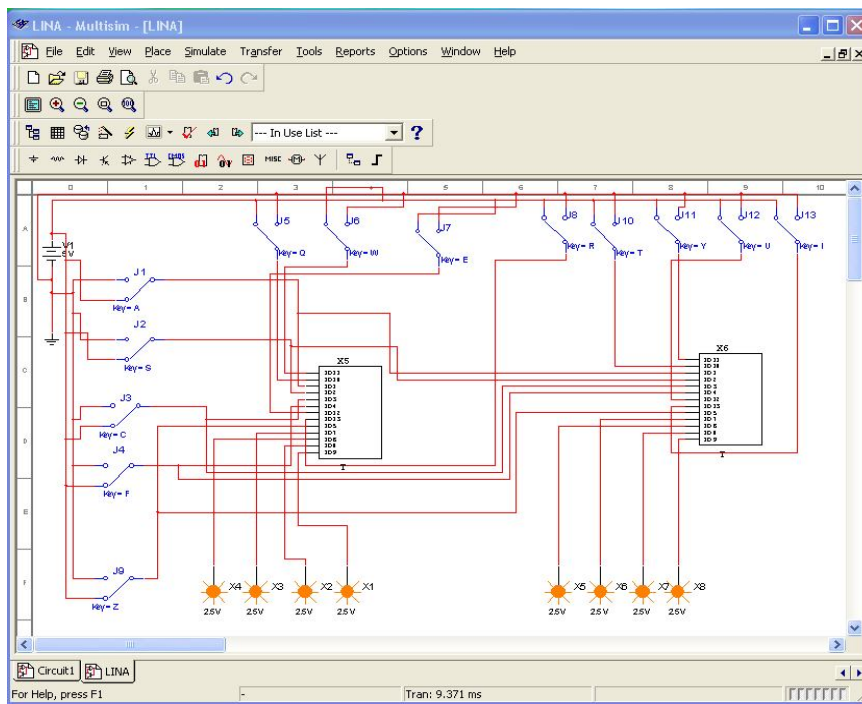
Fig. (12): 8*8 bit RAM from 8*4 bit RAM.
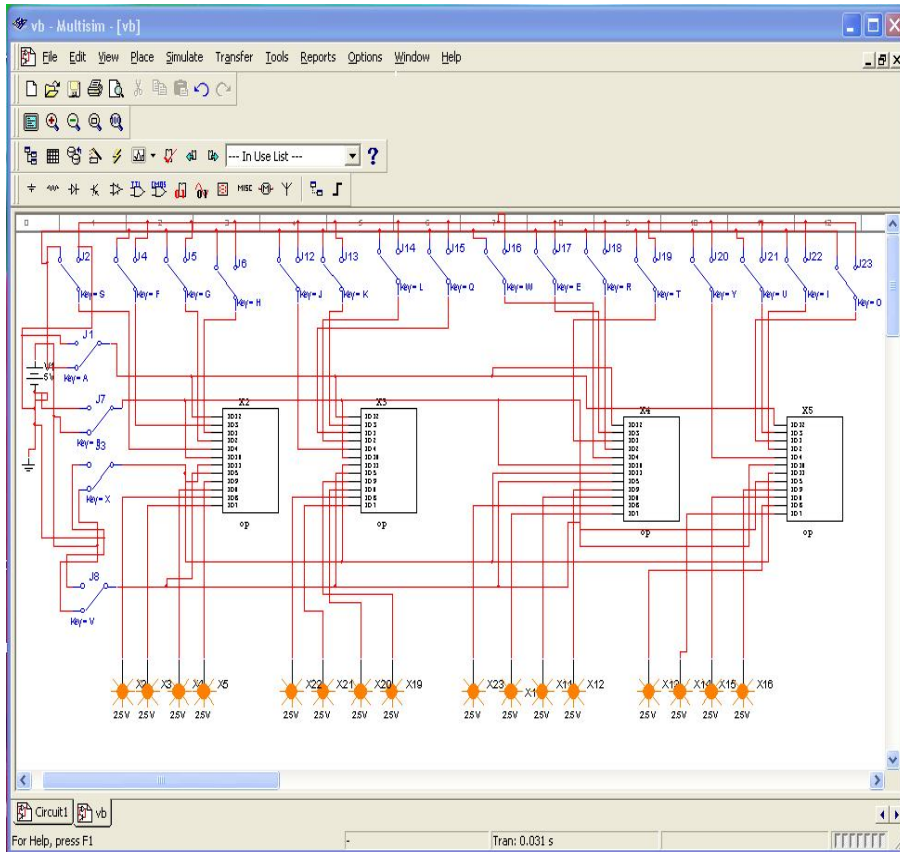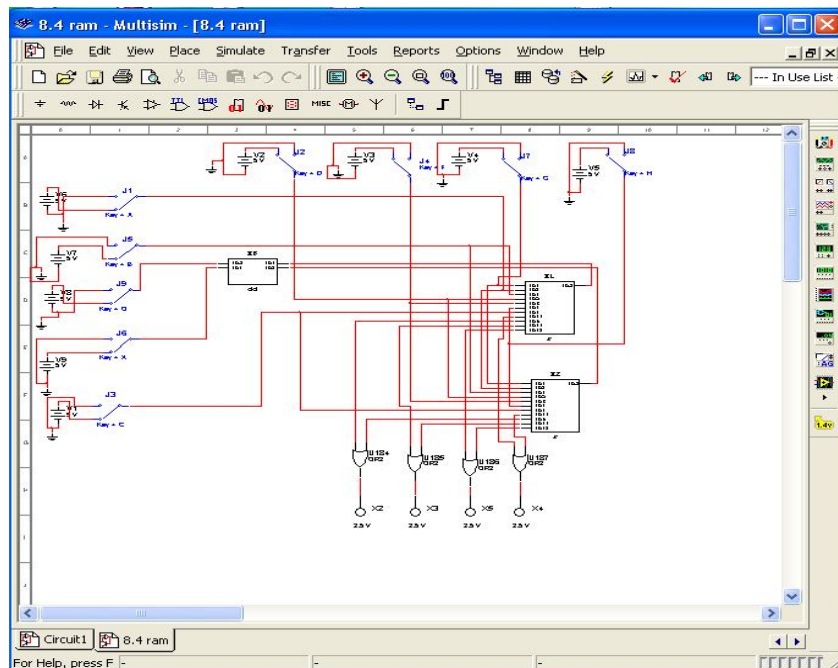
Fig. (13): 4*16 bit RAM from 4*4 bit RAM.
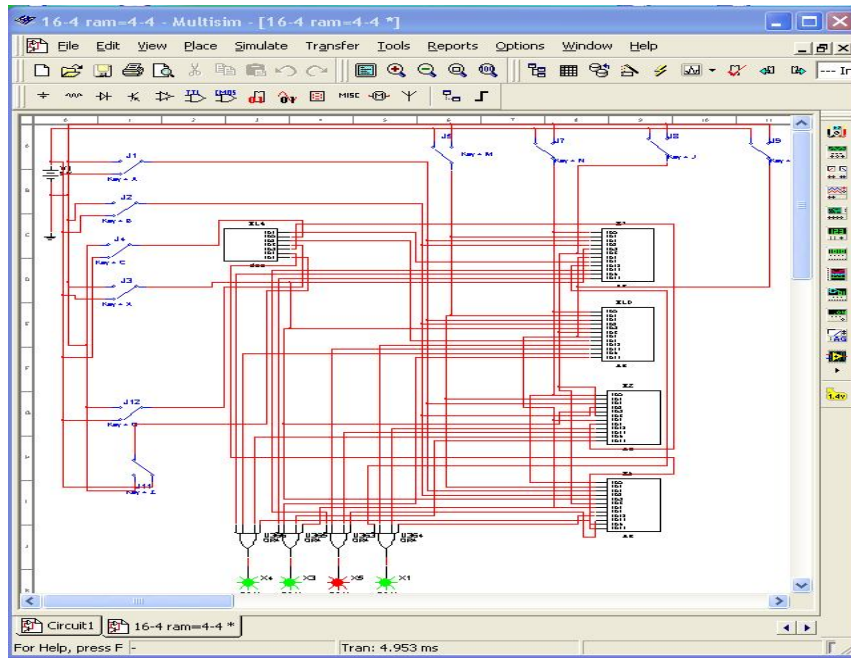

Fig. (14): 8*4 bit RAM from 4*4 bit RAM.

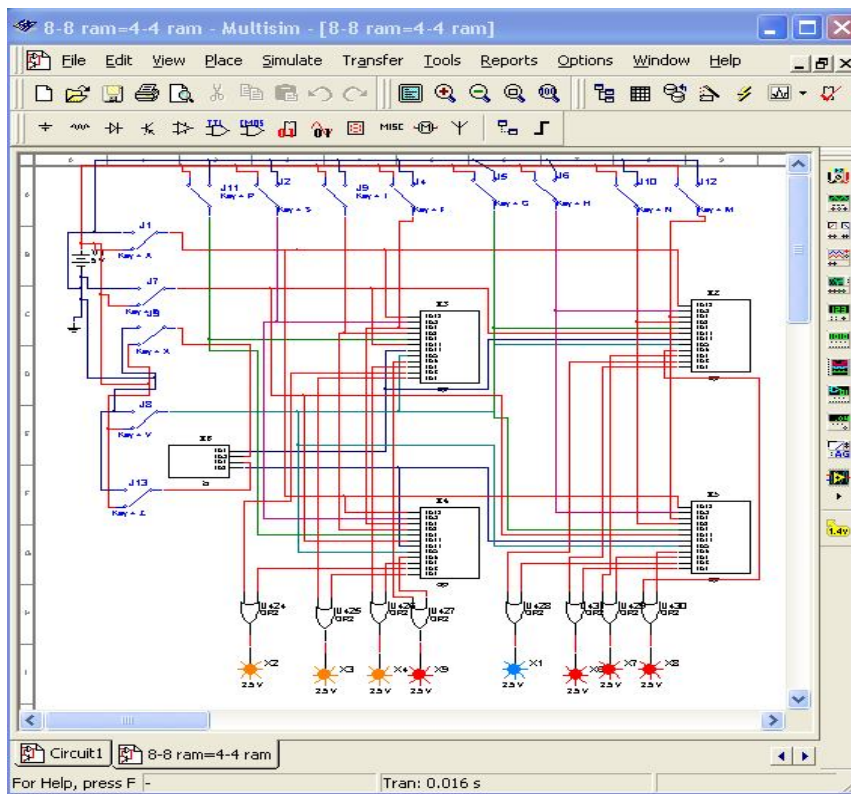**Fig.(15):** 16*4 bit RAM from 4*4 RAM.

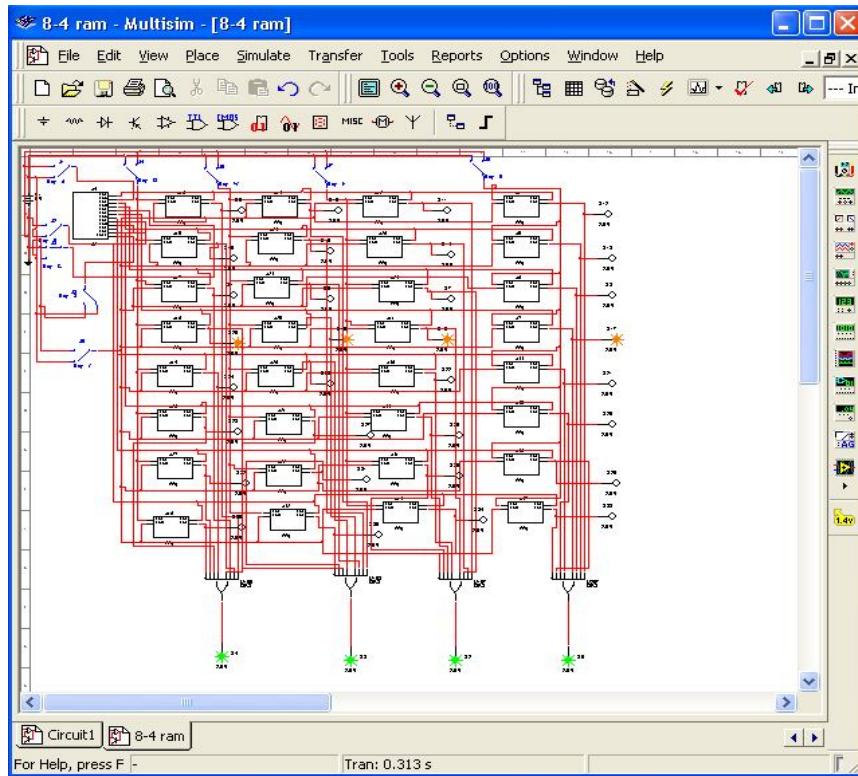**Fig. (16):** 8*8 bit RAM from 4*4 bit RAM.

Fig. (17): 8*4 bit RAM By using four chips of 4*4 bit RAM.

بناء أداة الخزن (ذاكرة القراءة العشوائية) باستخدام البرنامج التطبيقي (Multisim)

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الخلاصة:–

ذاكرةالقراءة العشوائية هي احد الأجزاء المهمة في العديد من الأنظمة كأنظمة الحاسوب والاتصالات وهناك العديد من البرامج التطبيقية المستخدمة لبناء الدوائر الرقمية لذاكرة القراءة العشوائية. في هذا المشروع، تم استخدام البرنامج التطبيقي (Multisim 9) لبناء ونمذجة العديد من الدوائر المنطقية لذاكرة القراءة العشوائية وبأحجام متعددة بحيث تم بناء ذاكرة (RAM) من ذاكرة (RAM) أخرى. كذلك تهيئة الذاكرة كجزء من أجزاء نظام الحاسوب المحمول جوا.